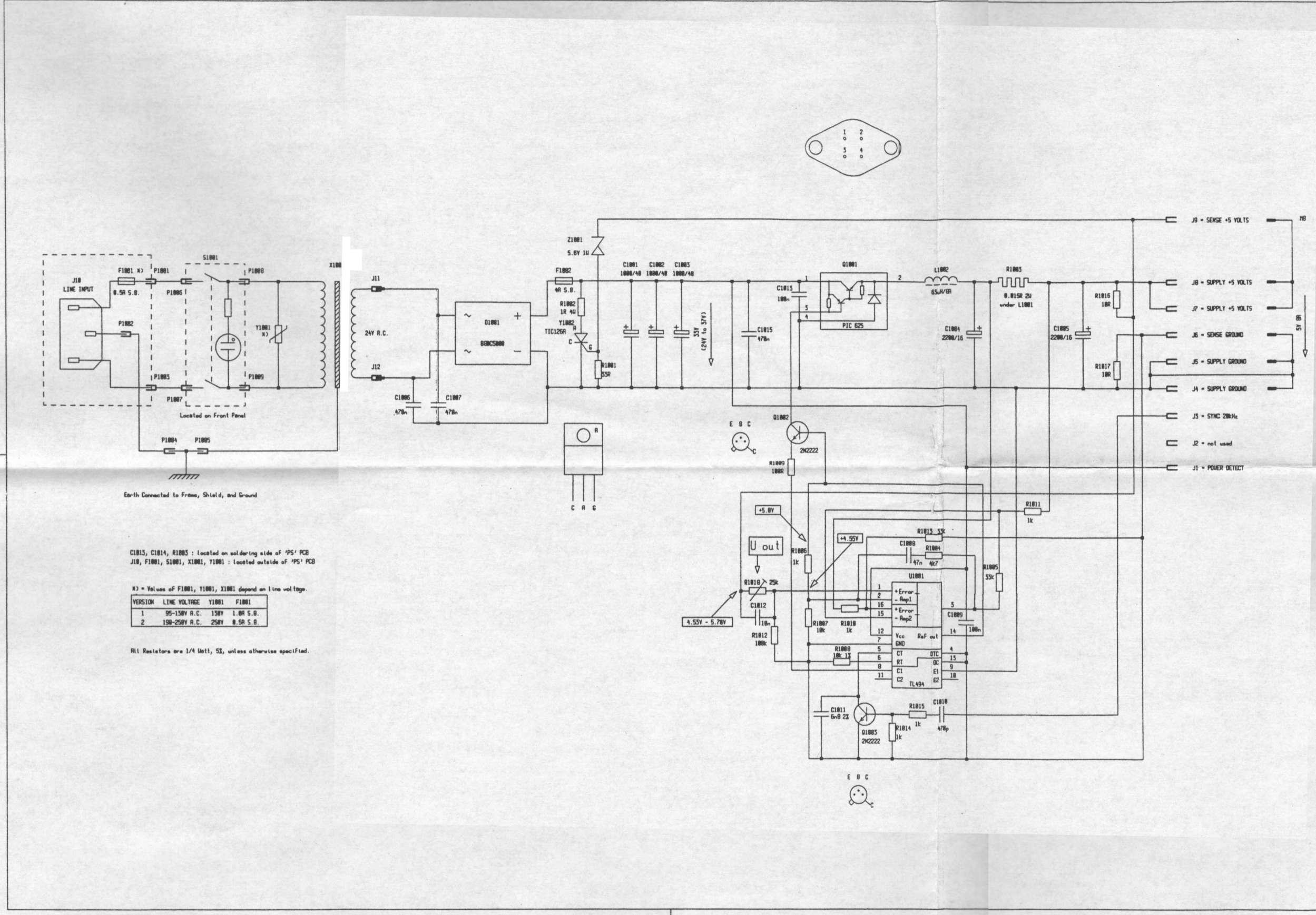


D

C

B

A



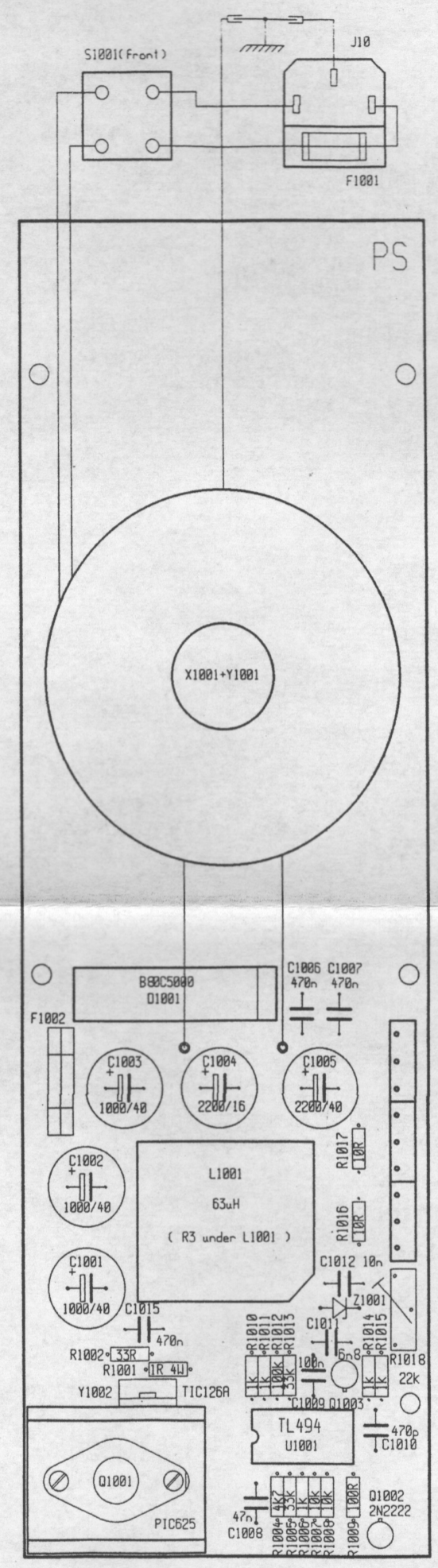
Earth Connected to Frame, Shield, and Ground

C1015, C1014, R1005 : Located on soldering side of 'PS' PCB  
 J10, F1001, S1001, X1001, Y1001 : Located outside of 'PS' PCB

R1 = Value of F1001, Y1001, X1001 depend on Line Voltage

VERSION	LINE VOLTAGE	Y1001	F1001
1	95-130V A.C.	150V	1.0M S.B.
2	130-230V A.C.	250V	0.5M S.B.

All Resistors are 1/4 Watt, 5%, unless otherwise specified.



X1001 = Line Transformer  
 120V or 240V to 24V

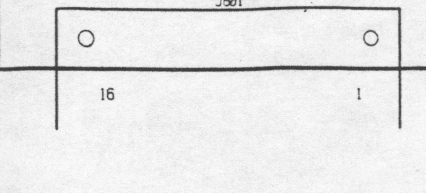
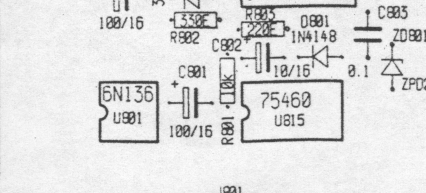
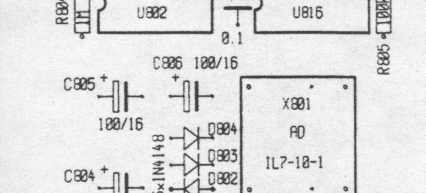
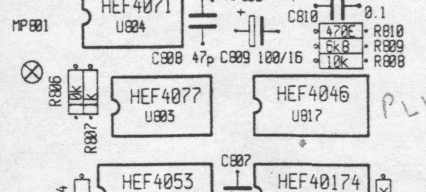
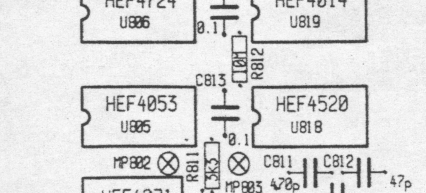
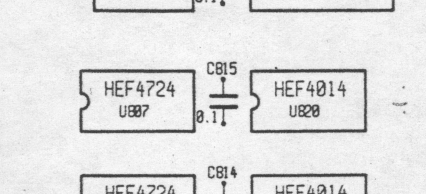
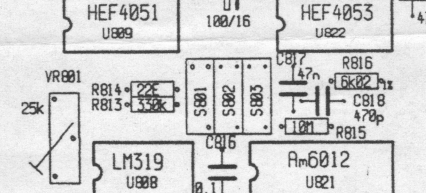
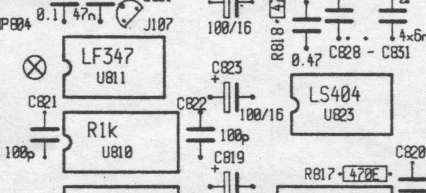
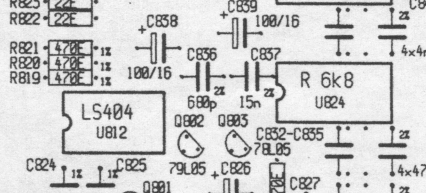
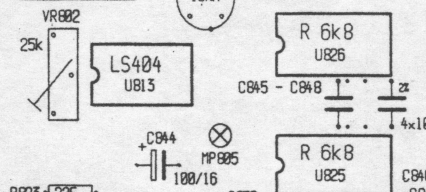
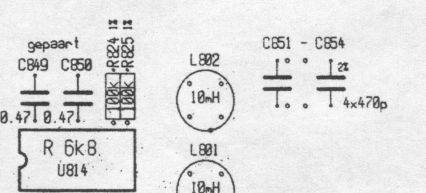
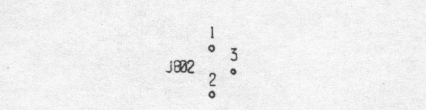
- J1 = POWER DETECT
- J2 = not used
- J3 = SYNC 20kHz
- J4 = SUPPLY GROUND
- J5 = SUPPLY GROUND
- J6 = SENSE GROUND
- J7 = SUPPLY +5 VOLTS
- J8 = SUPPLY +5 VOLTS
- J9 = SENSE +5 VOLTS

J1 to J9 = MOLEX Power Connector (Female)

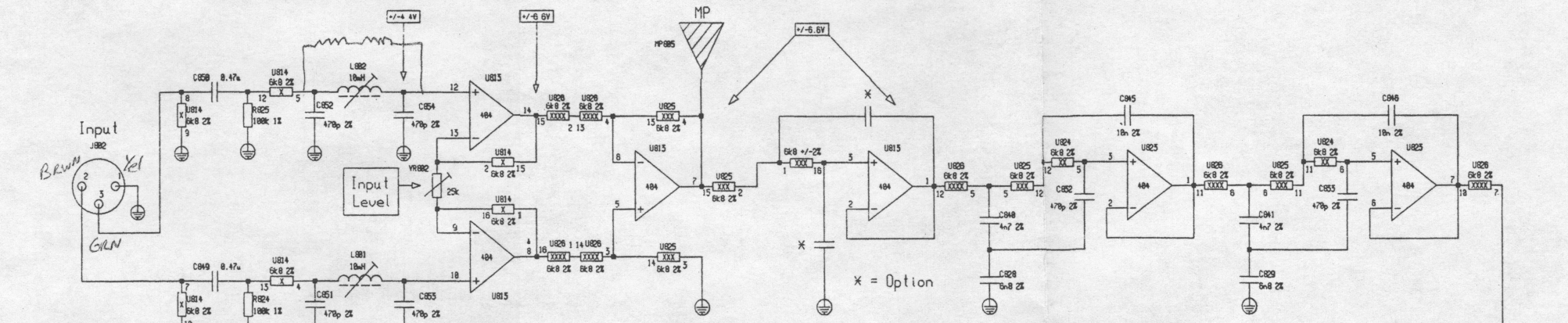
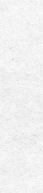
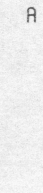
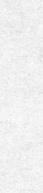
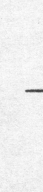
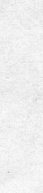
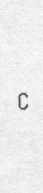
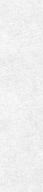
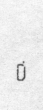
TOP ←  
 C1013 PS Front Panel C1014



AD

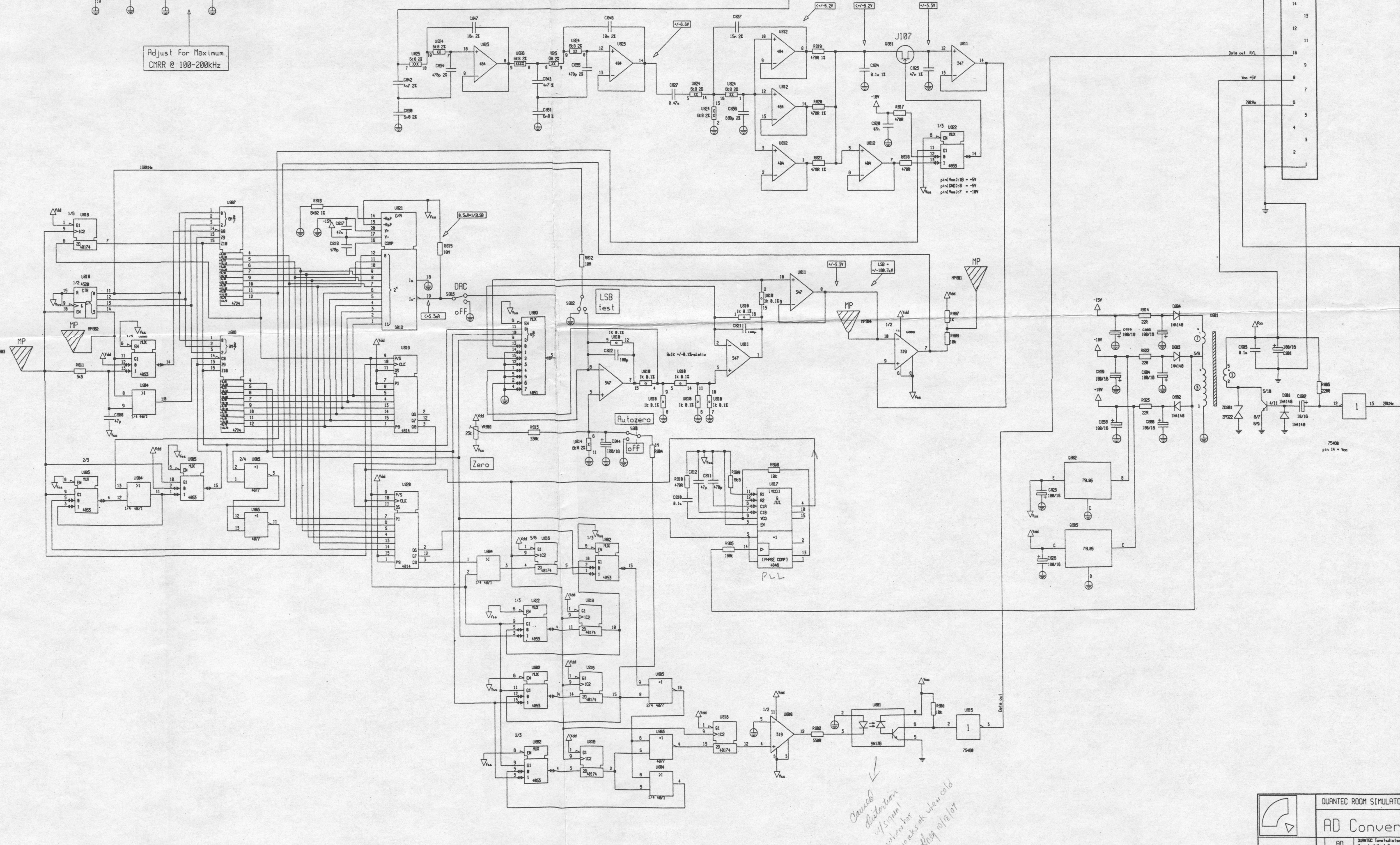


AD



Adjust for Maximum CMRR @ 100-200kHz

All OpAmp's: pin 11 = -10V  
pin 4 = +10V



DAC

LSB test

Autozero

Zero

PLL

Caused distortion  
with signal  
when hot  
works ok when cold  
Align mfr lot

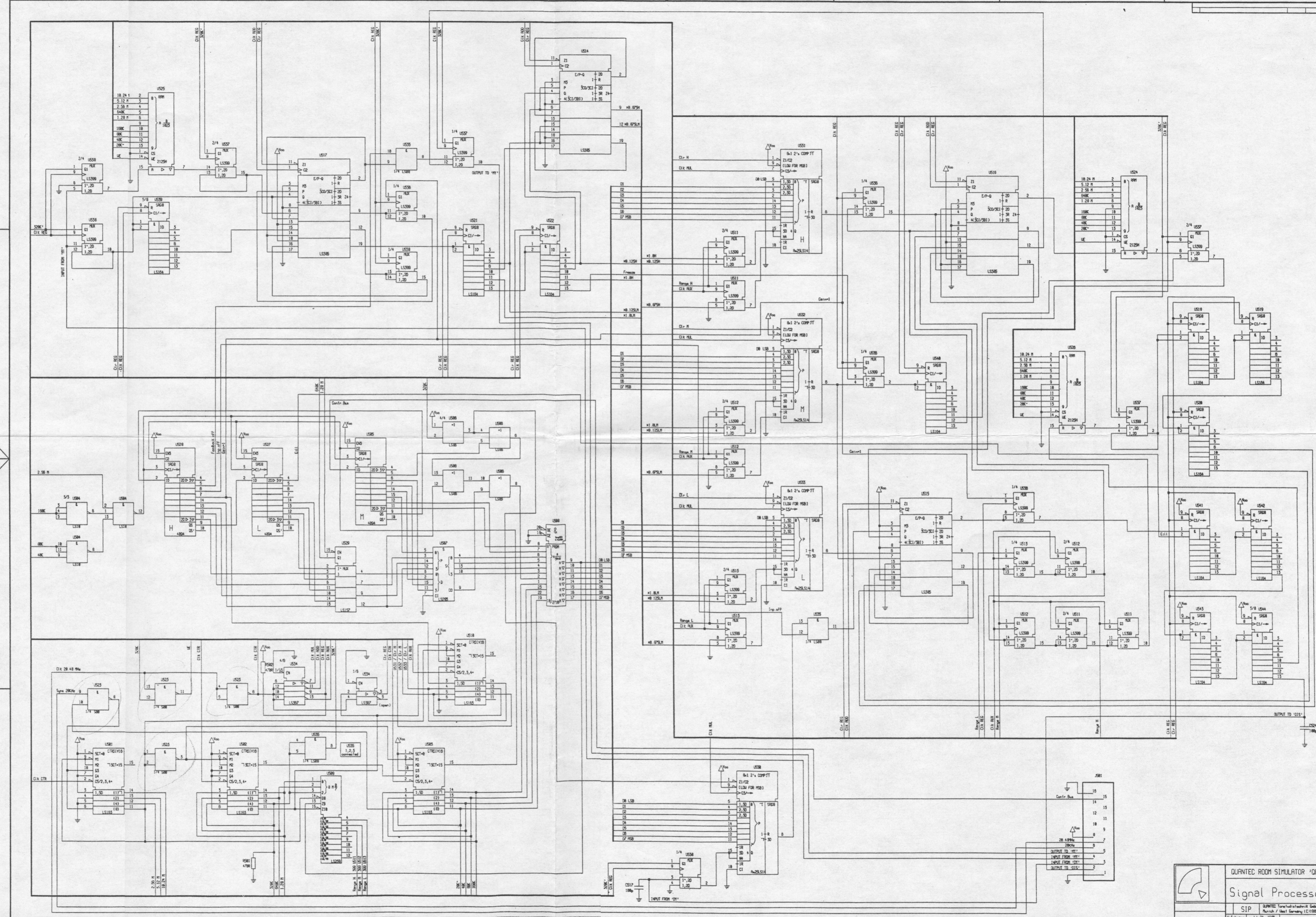
647

SIP

74LS164 U522	CS22	74LS164 U545
74LS164 U521	CS21	74LS164 U542
74LS164 U520	CS20	74LS164 U541
74LS164 U519	CS19	74LS164 U540
74LS164 U518	CS18	74LS164 U539
74LS385 U517	CS16	25LS399 U538
74LS385 U516	CS15	25LS399 U537
74LS385 U515	CS14	25LS399 U536
74LS385 U514	CS13	74LS08 U535
25LS399 U513	CS12	74LS367 U534
25LS399 U512	CS11	25LS14 U533
25LS399 U511	CS10	25LS14 U532
74LS163 U510	CS9	25LS14 U531
74LS259 U509	CS8	25LS14 U530
2716 U508	CS7	74LS157 U529
74LS283 U507	CS6	HEF4094 U528
74LS96 U506	CS5	HEF4094 U527
74LS10 U504	CS4	D2125H U526
74LS163 U503	CS3	D2125H U525
74LS163 U502	CS2	D2125H U524
74LS163 U501	CS1	74S00 U523

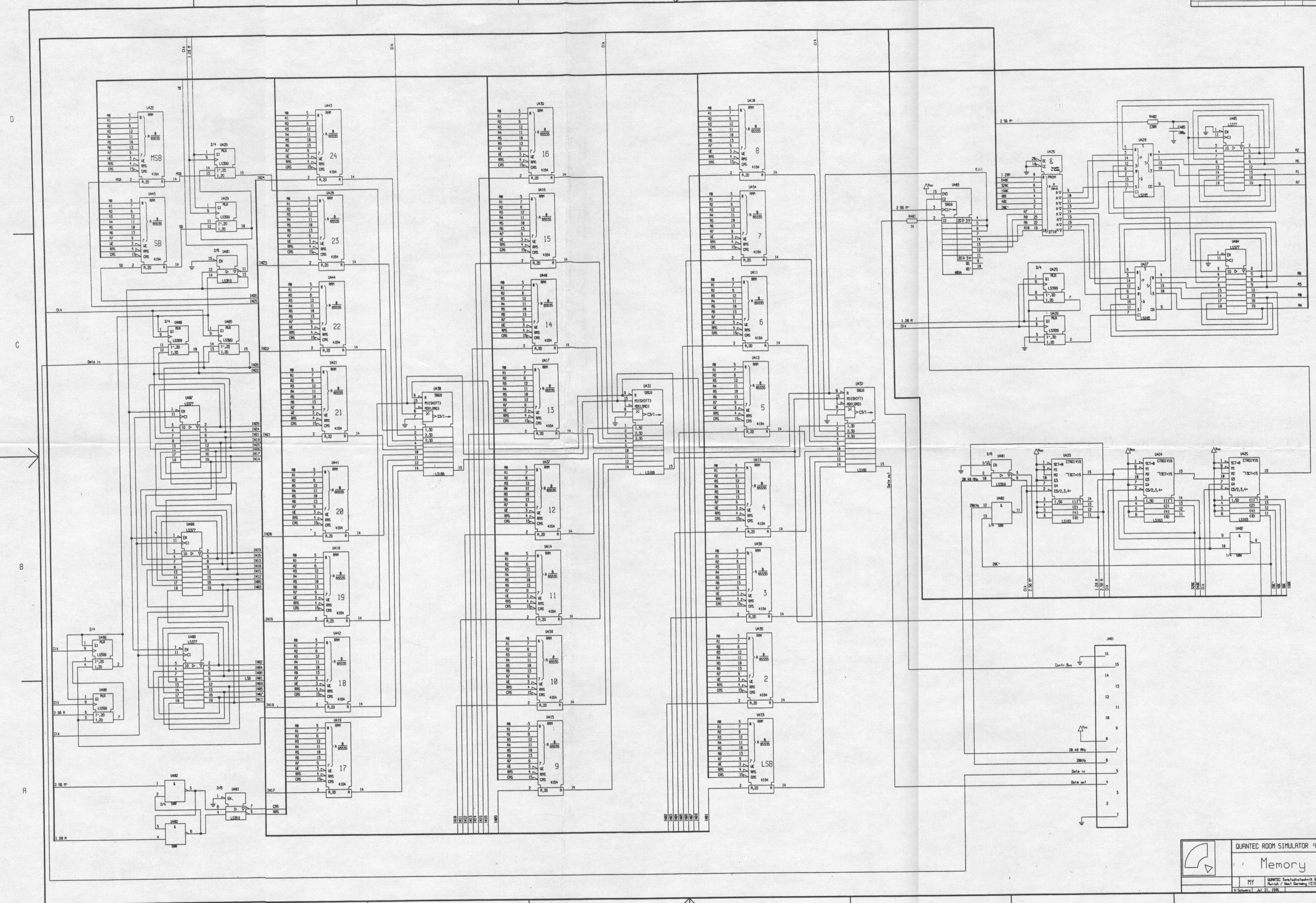
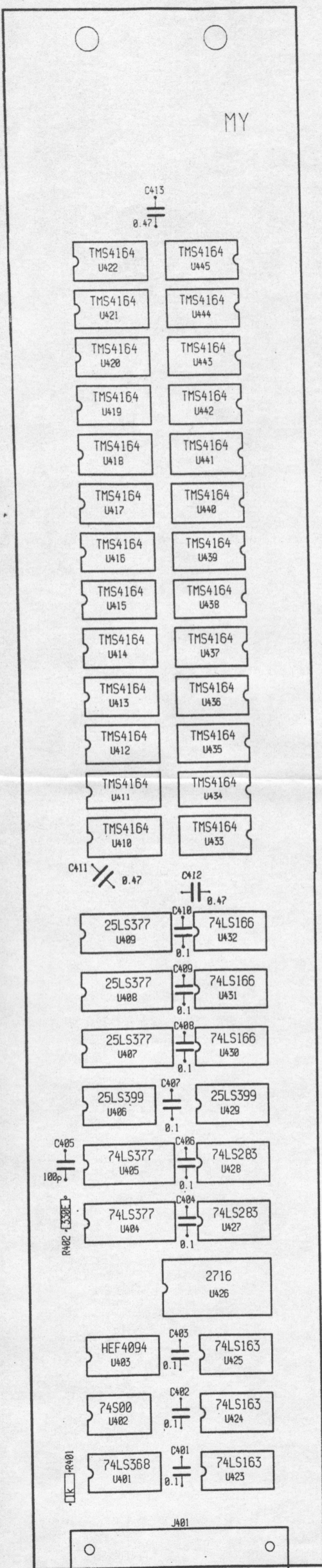
same EPROM for QRS and QRS1

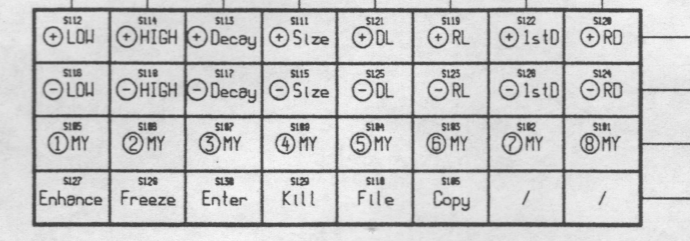
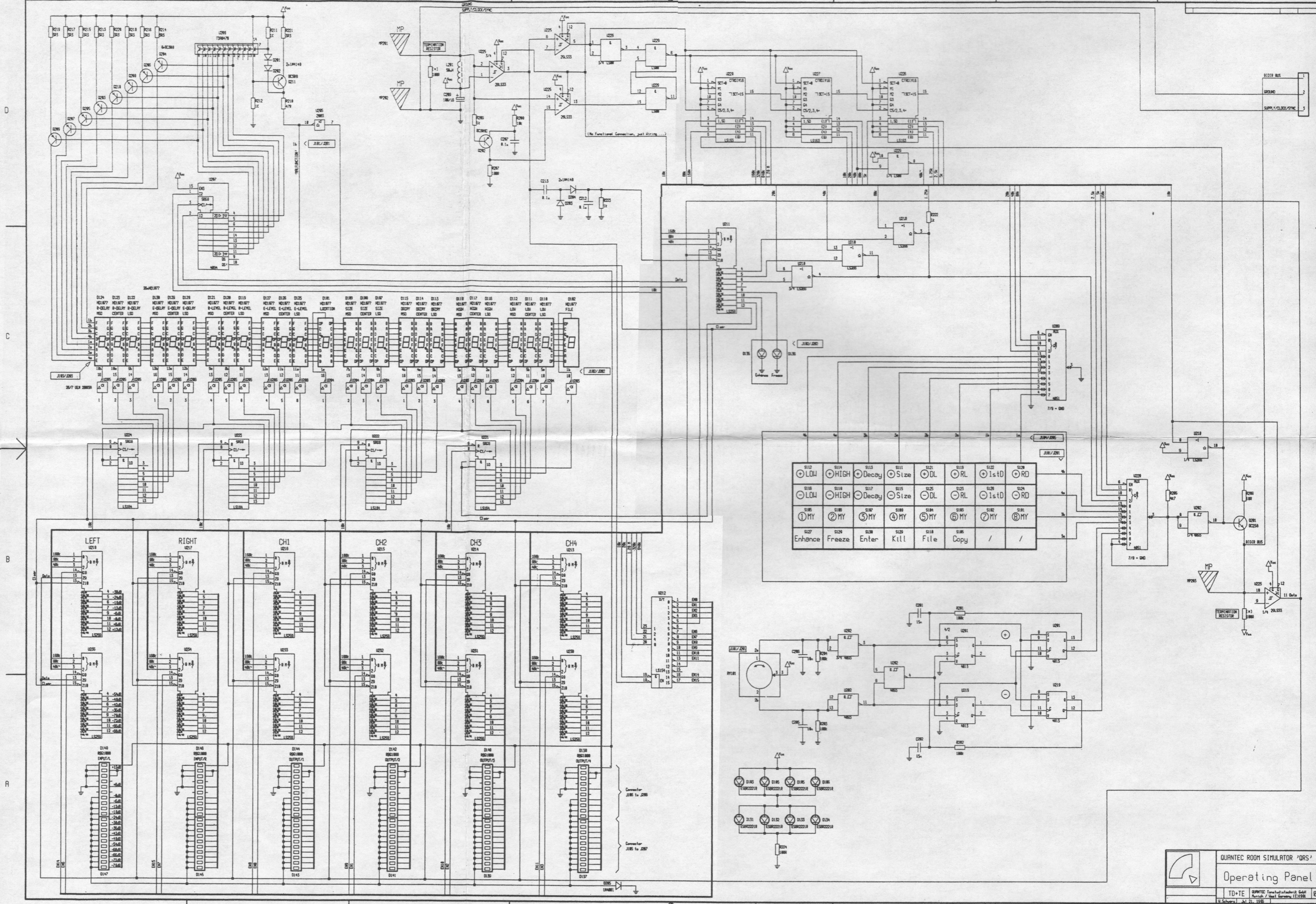
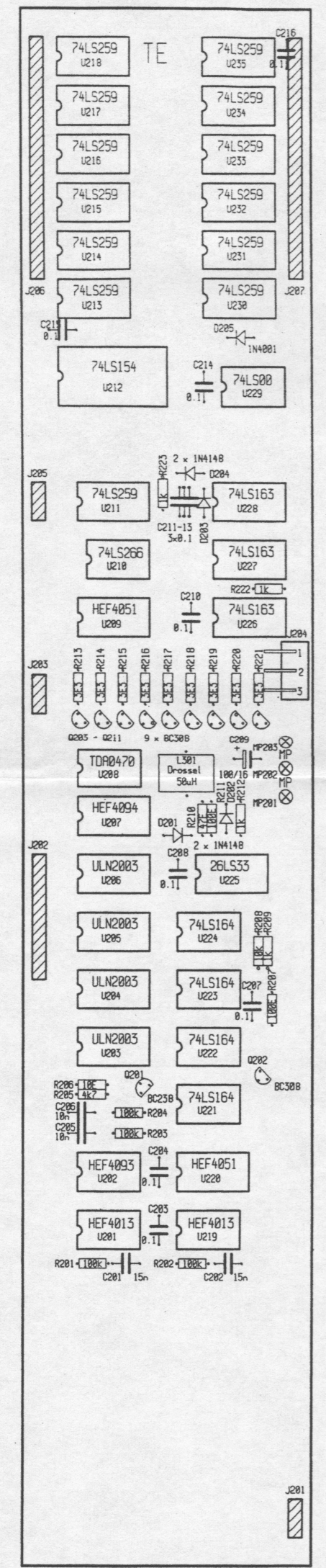
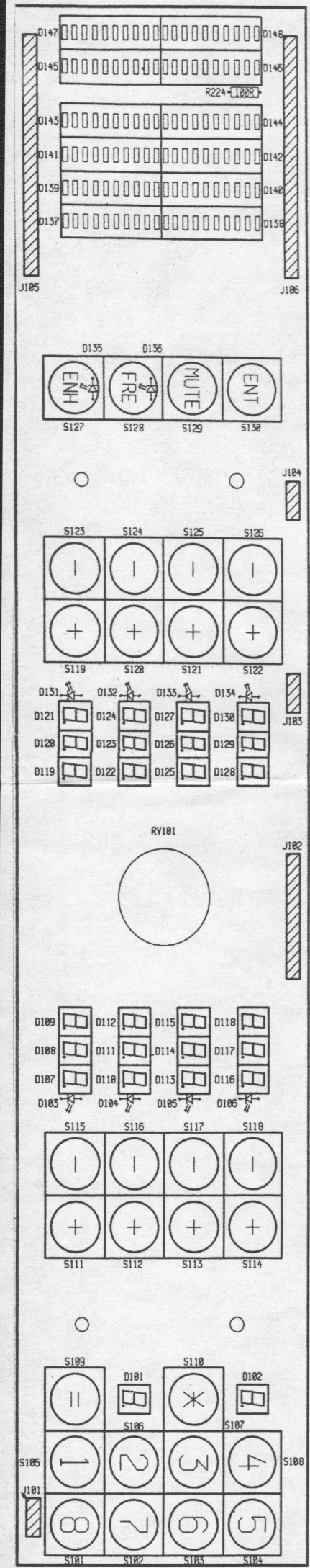
Caused massive drain when hot. Seemed like RAM issue but NO! 19Jul07

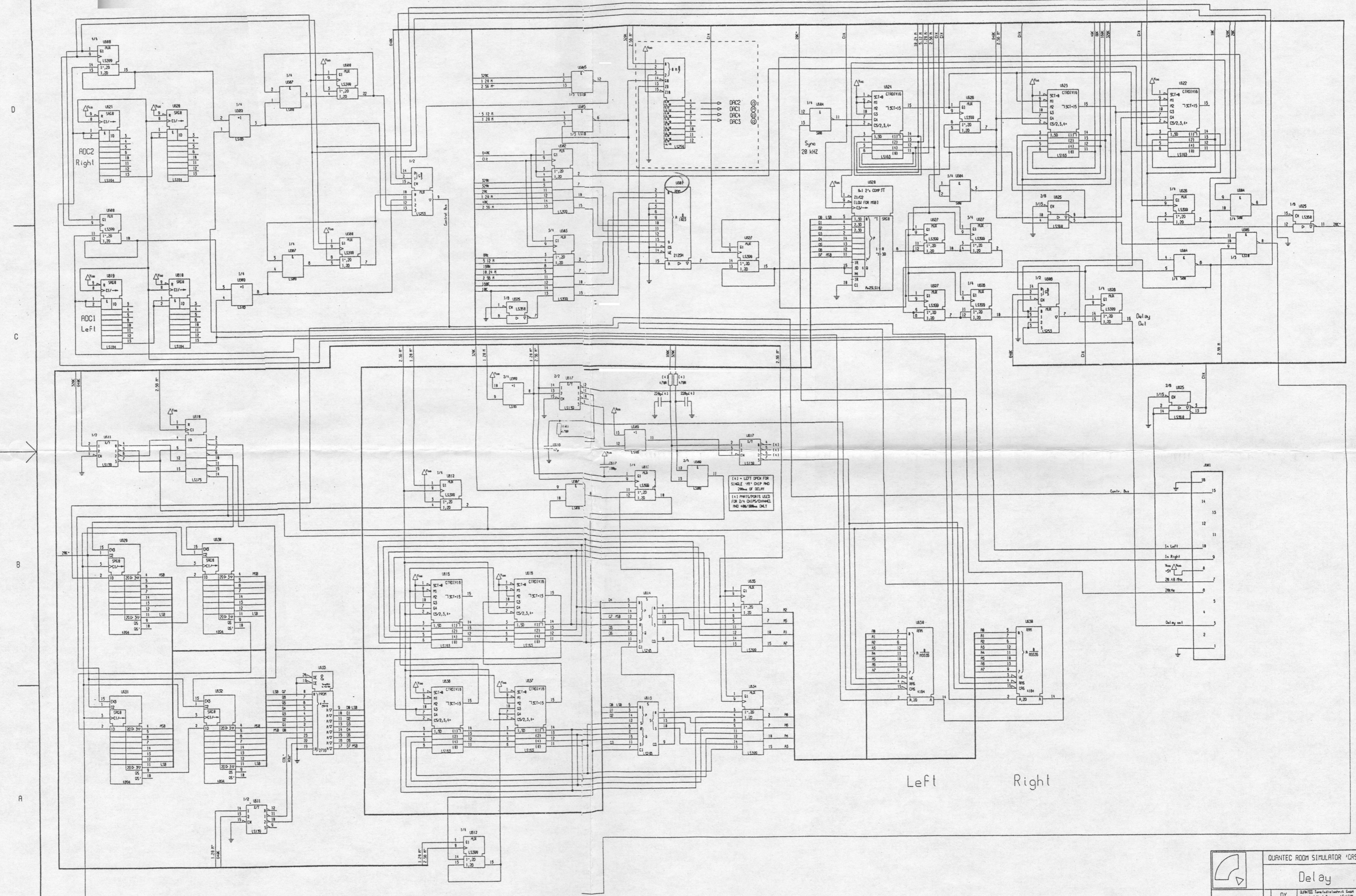
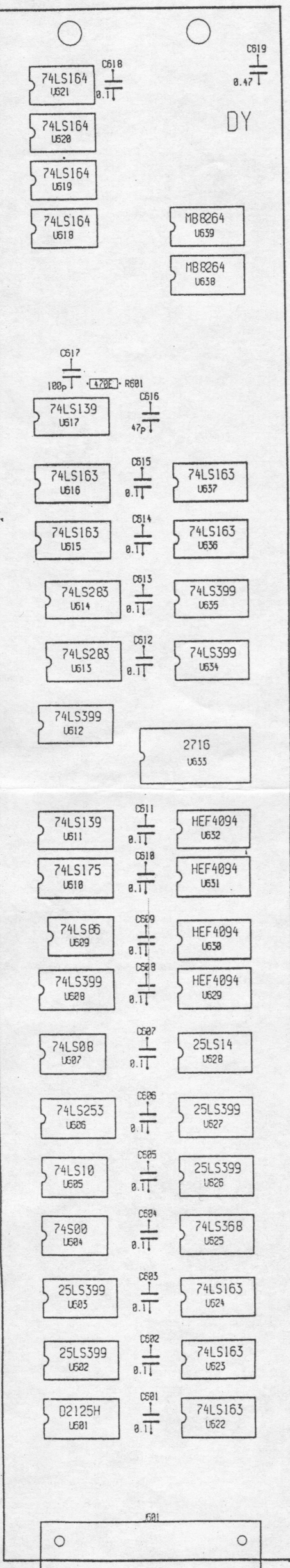


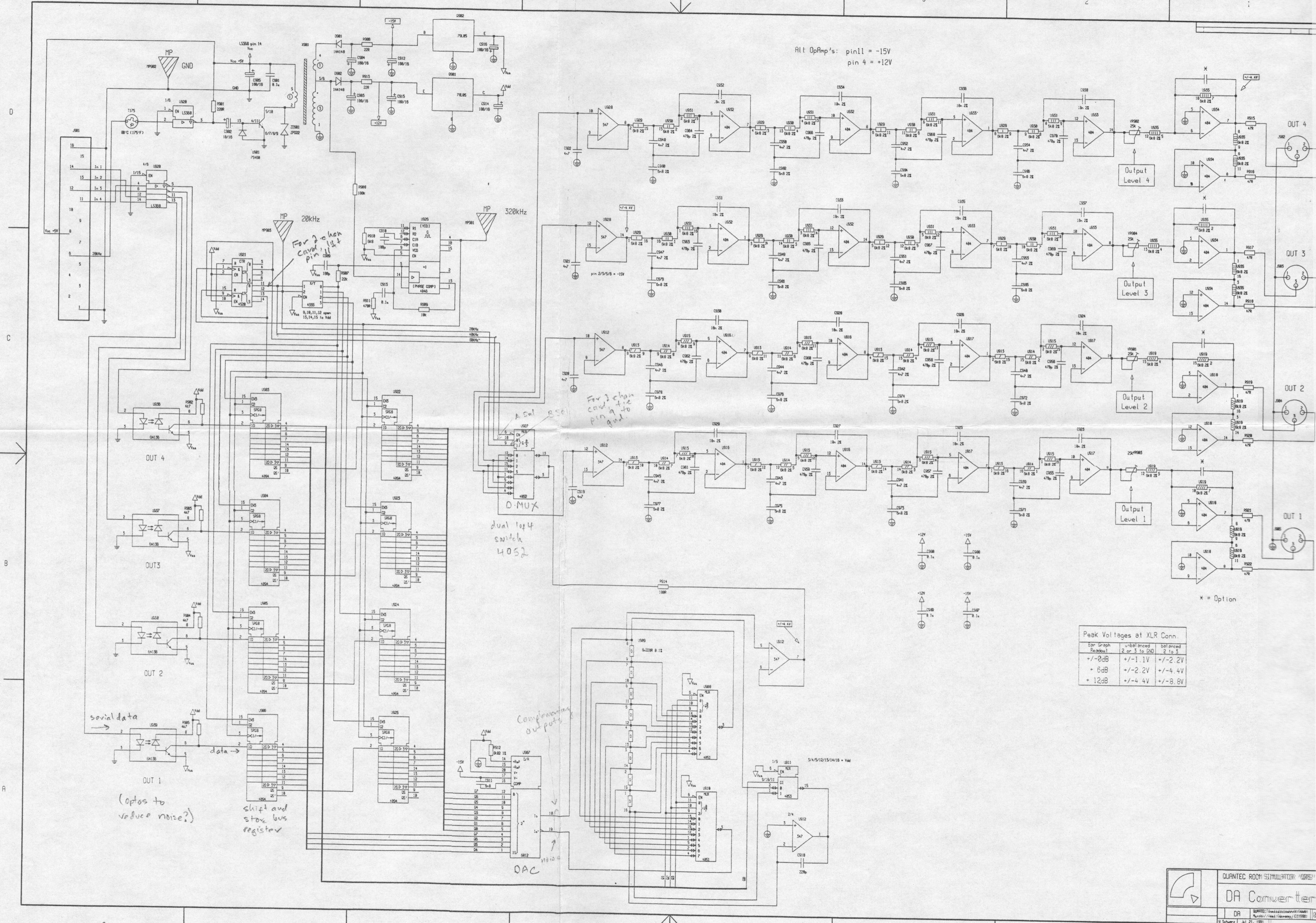
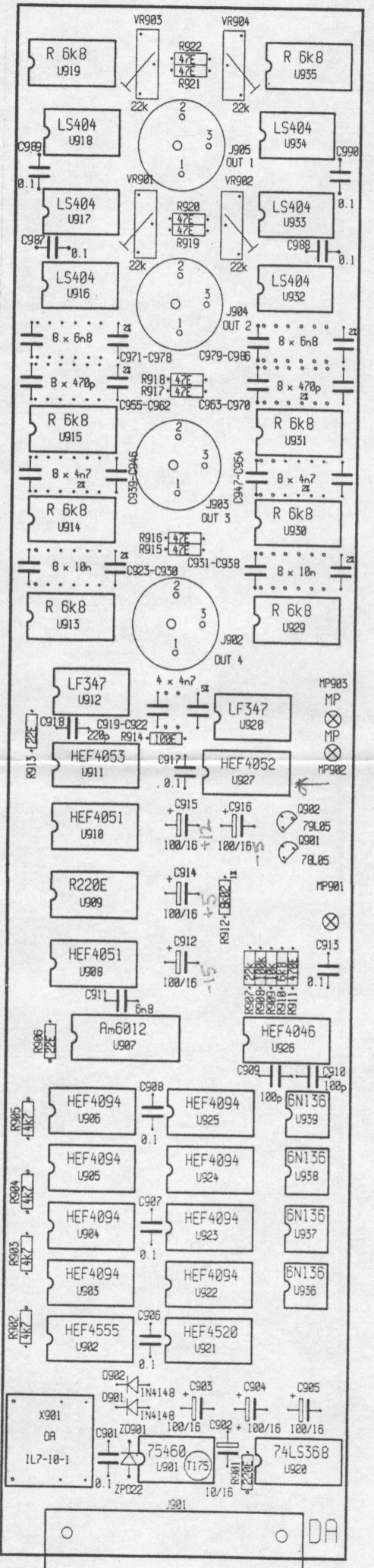
QUANTIC ROOM SIMULATOR 'QRS'  
Signal Processor  
SIP  
QUANTIC Tomtehofstrasse 6  
Ploching / West Germany D-11980  
U. Schwanz Jul. 21, 1988

3









All OpAmp's: pin11 = -15V  
pin 4 = +12V

Peak Voltages at XLR Conn.

Gain	unbalanced	balanced
-20dB	+/-1.1V	+/-2.2V
+6dB	+/-2.2V	+/-4.4V
+12dB	+/-4.4V	+/-8.8V

serial data →  
data →  
OUT 1  
(optos to reduce noise?)

shift and store bus register

DAC

D-MUX  
dual 4x4 switch  
4052

For 2 chan  
convert the  
pin 11 to  
pin 4

For 2 chan  
convert the  
pin 11 to  
pin 4

\* = Option



DIS

Quad output - U723 74LS86 must be installed  
- S703 strapped IN phase (Pin 10 U722 to pin 3 U718)

Stereo output - Remove U723  
- Short U723 pins 6+7 8+9 11+12 - tie 11+12 to pin 7  
(pin 7 is ground) S703 strapped out of phase pin 10 U722 to pin 2 U718

74LS253 U712	C712	0.1T
74LS377 U711	C711	0.1T
74LS86 U718	C710	0.1T
74LS86 U722	C709	0.1T
74LS00 U709	C708	0.1T
74LS385 U708	C707	0.1T
74LS399 U719	C706	0.1T
27S05 U706	C705	0.1T
74LS175 U718	C704	4.7p
74S374 U705	C703	0.1T
74LS163 U717	C702	0.1T
74LS163 U704	C701	0.1T
74LS163 U705	C700	0.1T
74LS253 U715	C699	0.1T
74LS163 U702	C698	0.1T
74LS32 U714	C697	0.1T
74LS368 U701	C696	0.1T
74LS164 U713	C695	0.1T

