SERVICE MANUAL
& PARTS LIST (without price)

SAMPLING SYNTHESIZER MODULE

FZ-20M

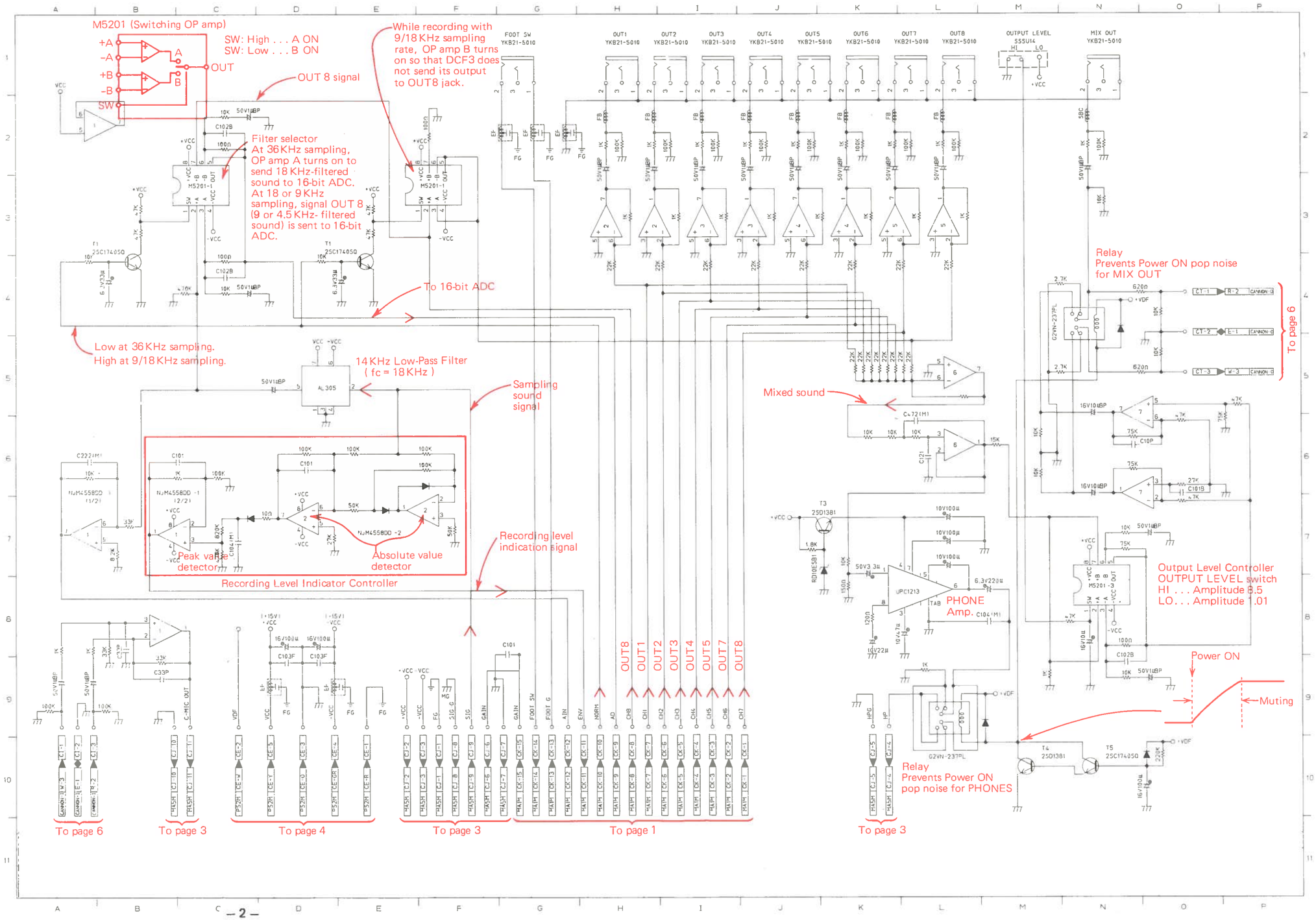
MAR. 1989

FZ-20M

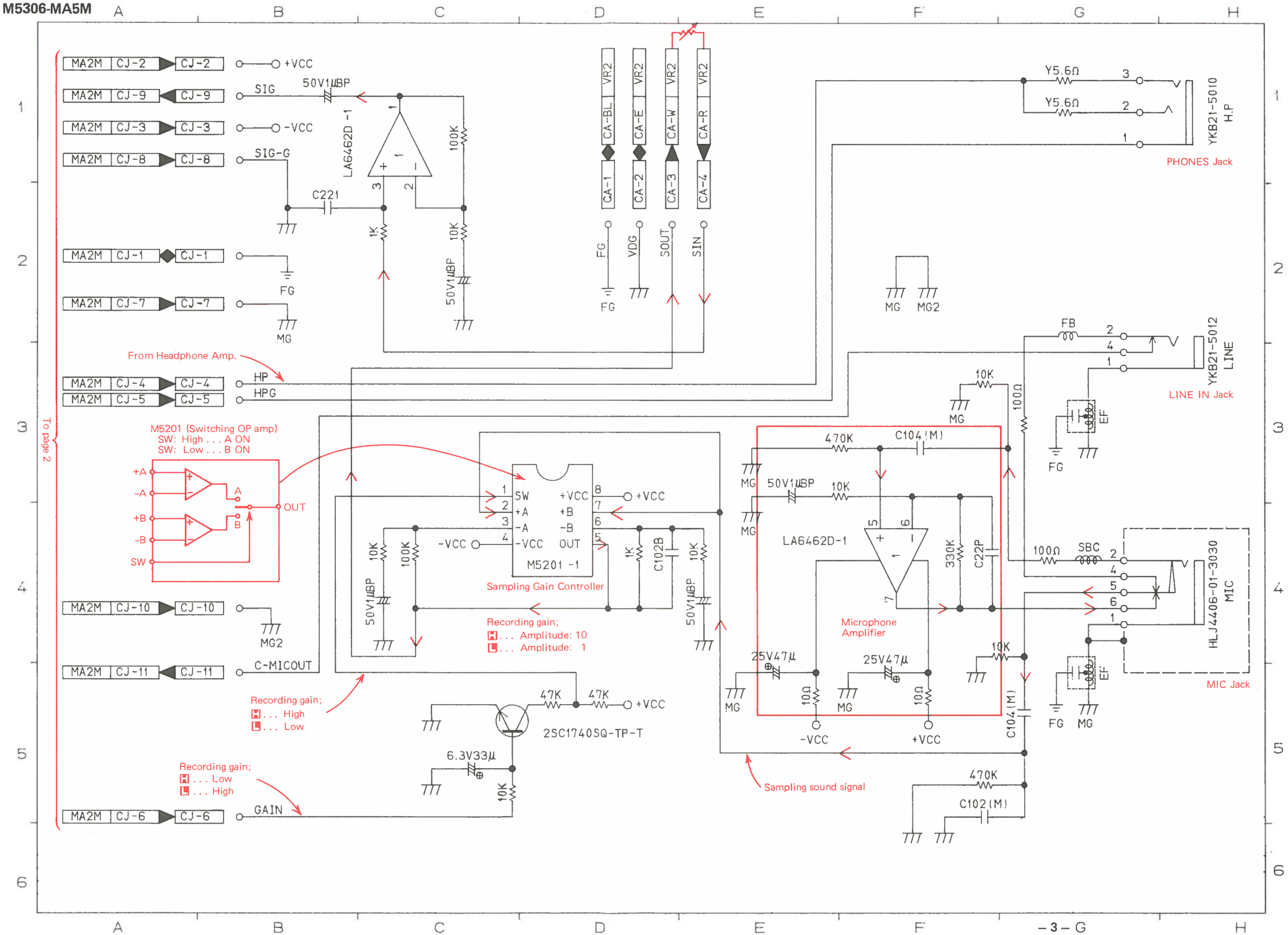
CASIO®

CONTENTS

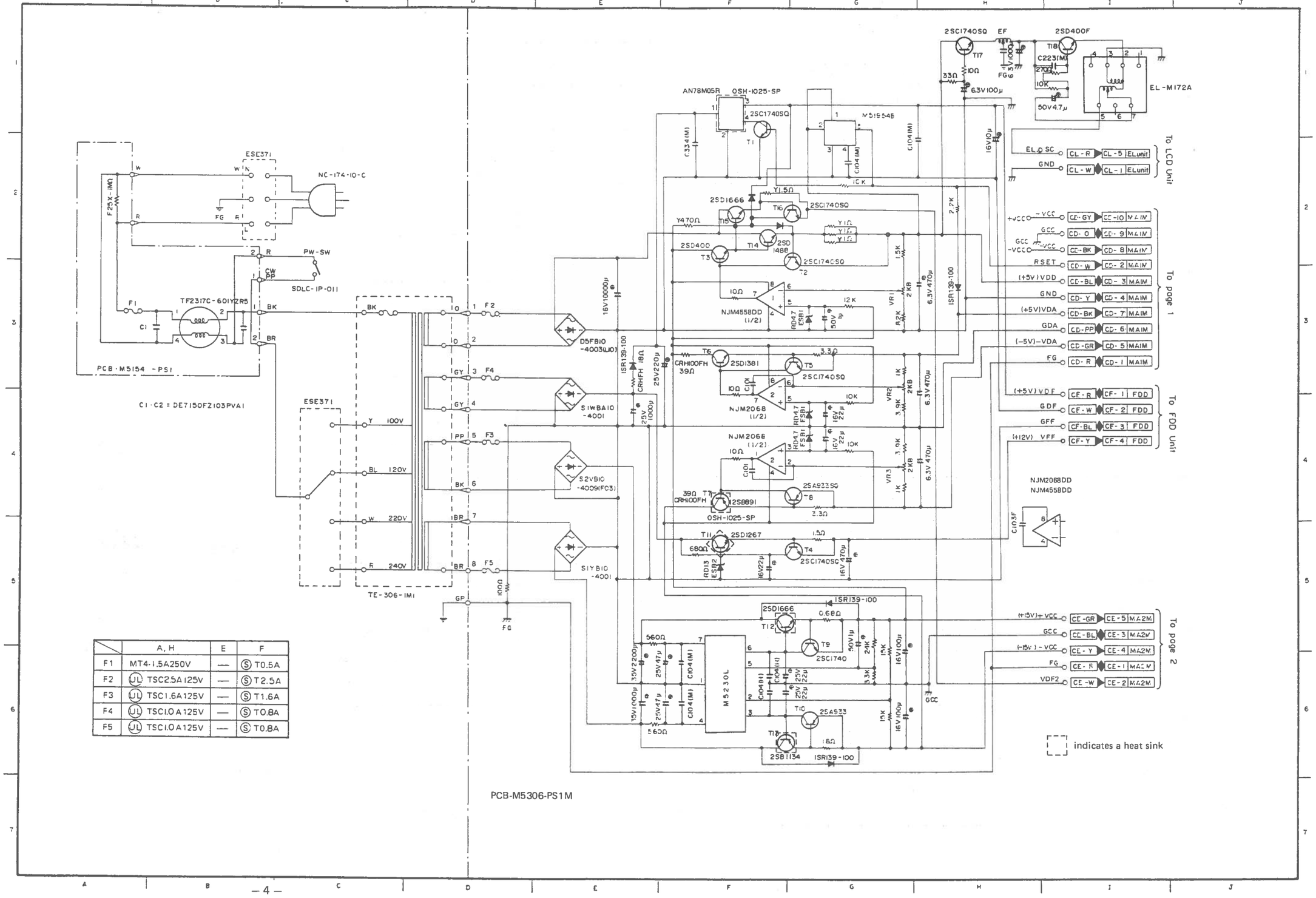
2. PCB M5306-MA2M



3. PCB M5306-MA5M



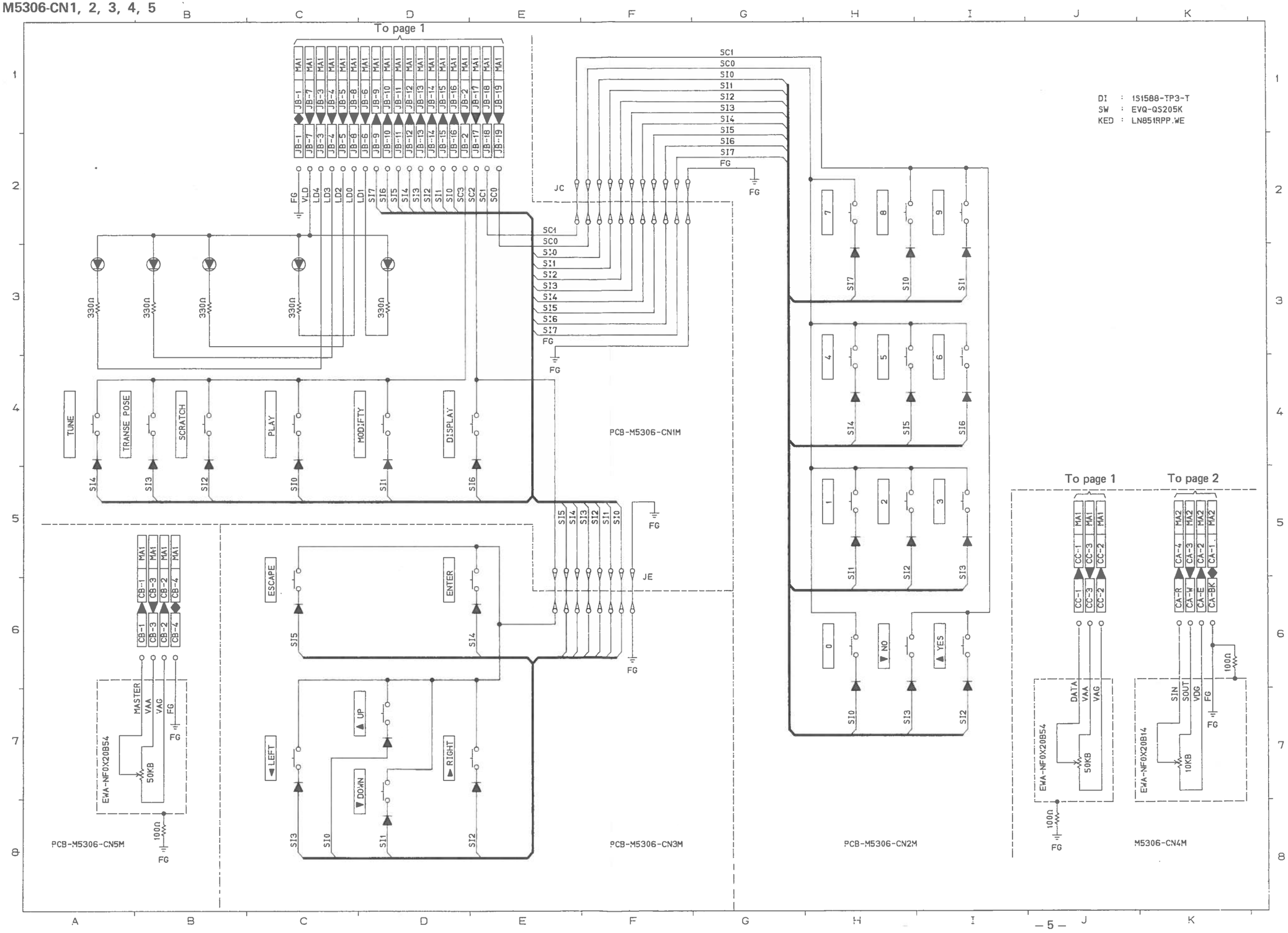
4. PCB M5306-PS2M



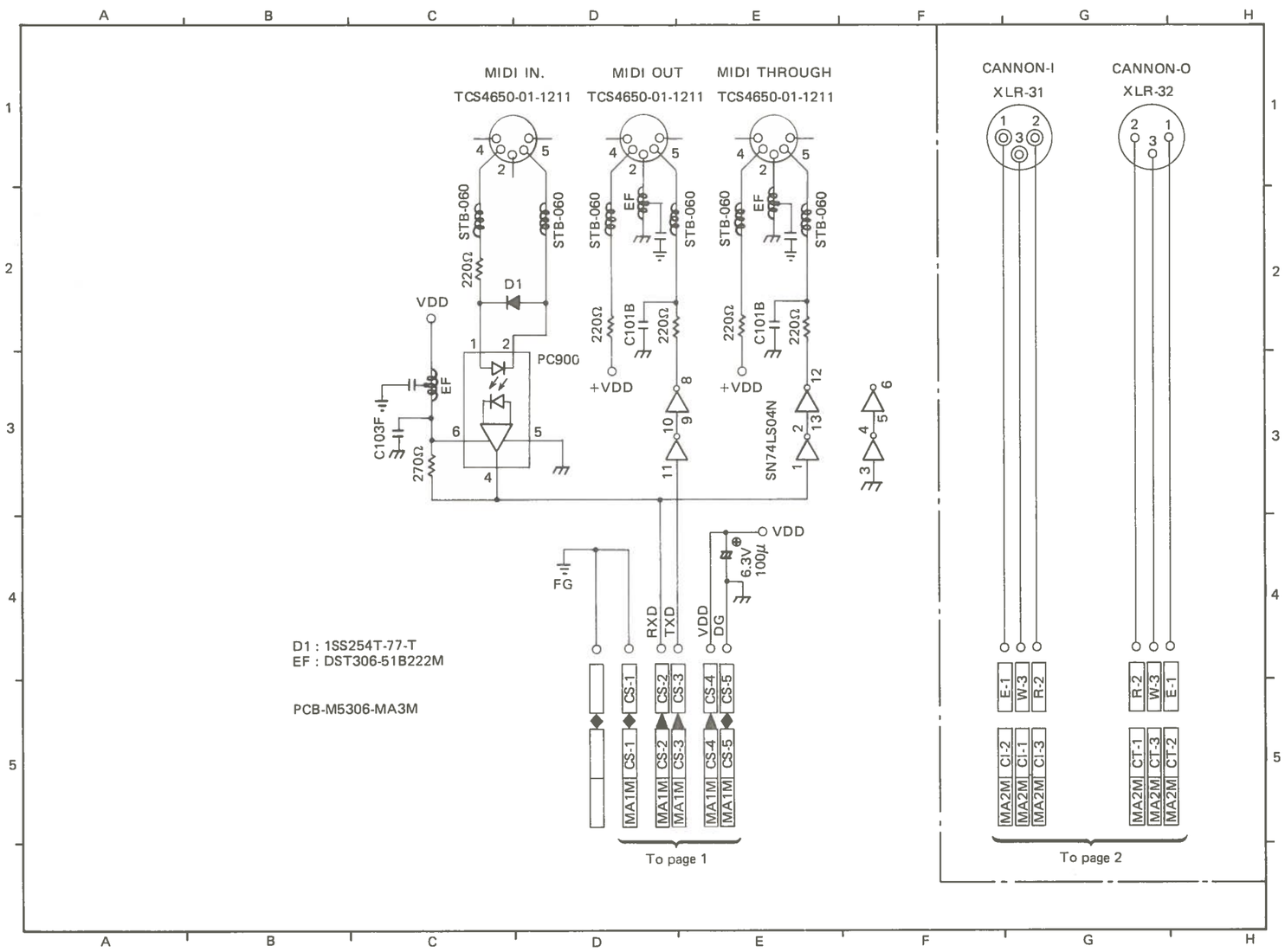
	A, H	E	F
F1	MT4-1.5A250V	—	Ⓢ T0.5A
F2	Ⓤ TSC2.5A125V	—	Ⓢ T2.5A
F3	Ⓤ TSC1.6A125V	—	Ⓢ T1.6A
F4	Ⓤ TSC1.0A125V	—	Ⓢ T0.8A
F5	Ⓤ TSC1.0A125V	—	Ⓢ T0.8A

PCB-M5306-PS1M

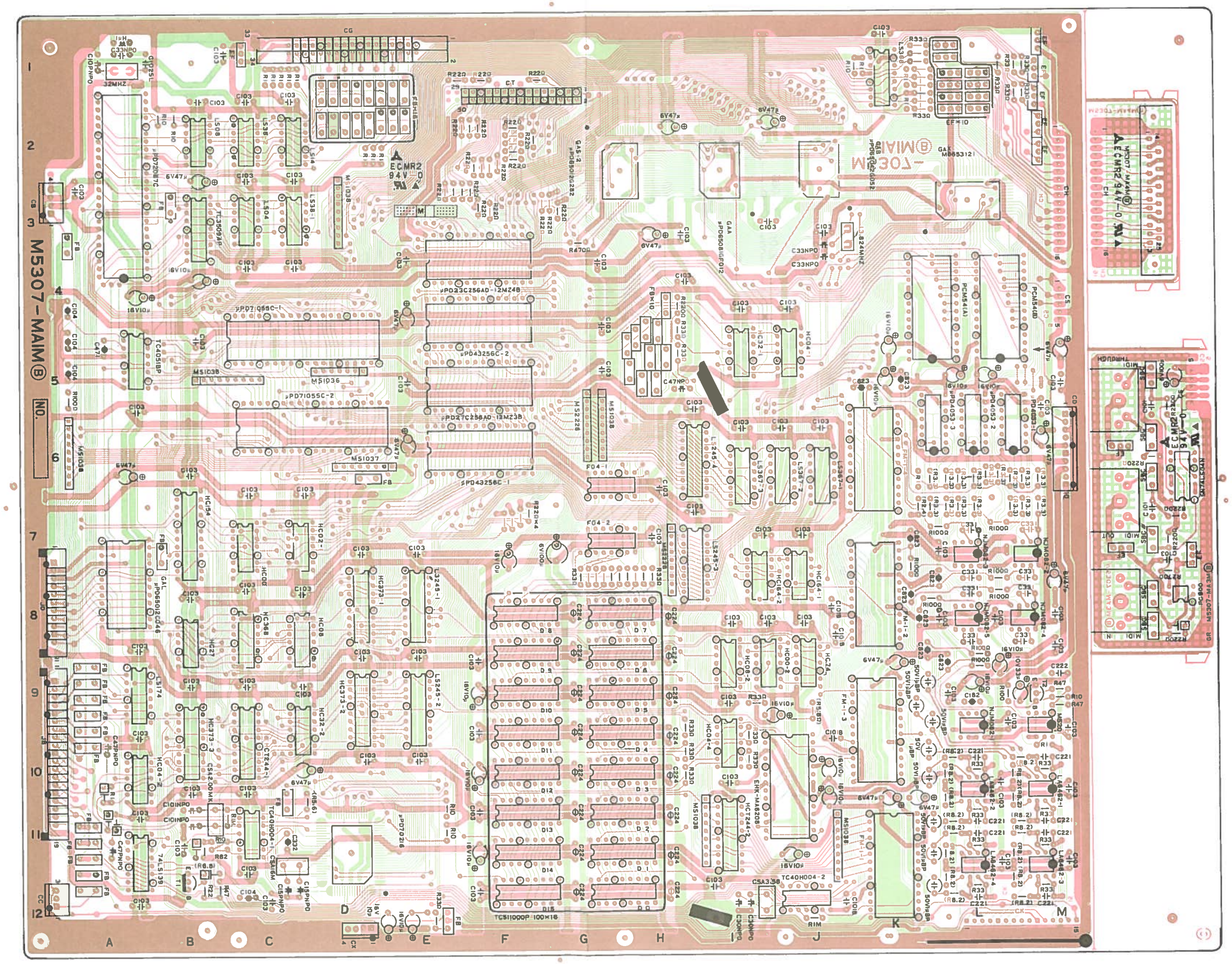
5. PCBs M5306-CN1, 2, 3, 4, 5



6. PCB M5306-MA3M



PCB VIEW



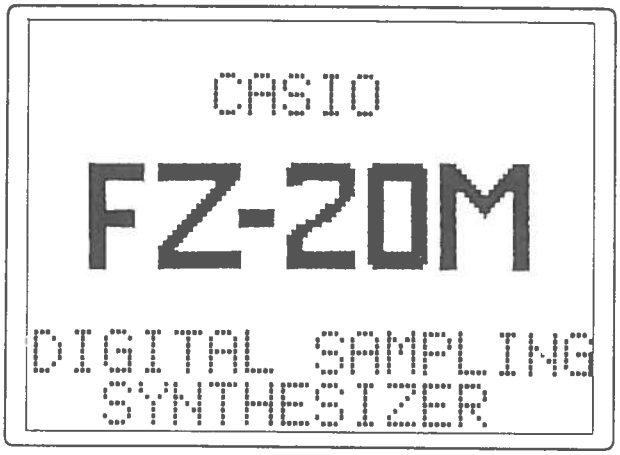
OUTLINE OF DIAGNOSTIC PROGRAM

FZ-20M's each device can be checked by the built-in program or diagnostic floppy disk.

Devices to be Checked	Checking Method	Program Area
SYSTEM ROM	64K byte check sum	Automatically checked at Power ON
SYSTEM RAM		Automatically checked at Power ON
FDC	Physical read/write of certain track or sector of a floppy disk	Built-in Program
LCD	All the dots and the characters are displayed	Built-in Program
Hard Disk	Read/Write check of Hard Disk	Diagnostic Floppy Disk
WAVE MEMORY RAM	Indicates a faulty RAM number	Diagnostic Floppy Disk
Switches LEDs Pedal Switch	By pressing the switches in order, functions of the switches and LEDs are checked.	Diagnostic Floppy Disk
Keys	Hit key's number, velocity, after touch values of external keyboard are indicated.	Diagnostic Floppy Disk
Pitch Bender Modulator Volume Pedal Main Volume	Indicates control values of external keyboard.	Diagnostic Floppy Disk
FZ-20M's voice circuit	FZ-20M's button provides sound	Diagnostic Floppy Disk

* Head cleaning and alignments (Cat's eye, burst, read level etc.) can be performed at FDC checking

SYSTEM ROM/RAM CHECK



When System ROM and RAM function properly, the LCD indicates the figure shown on the left a few seconds after Power ON.

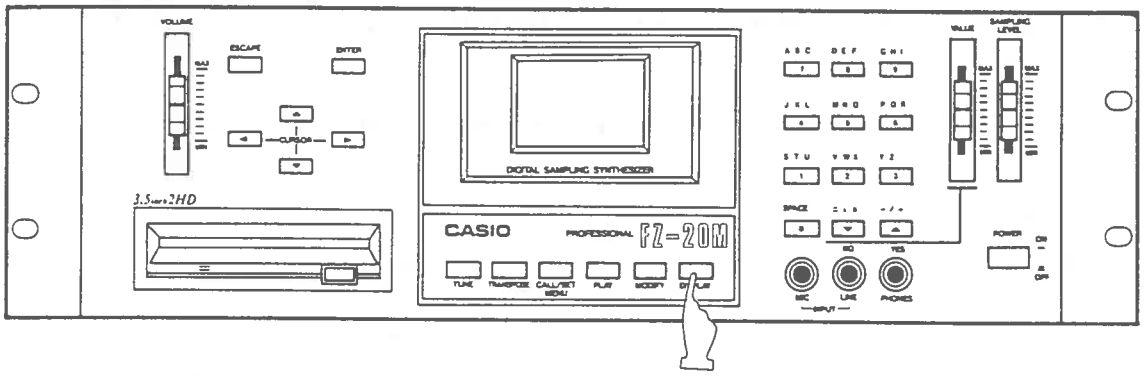
If System ROM or RAM is faulty, the LCD indicates so.

SELF DIAGNOSTIC PROGRAM

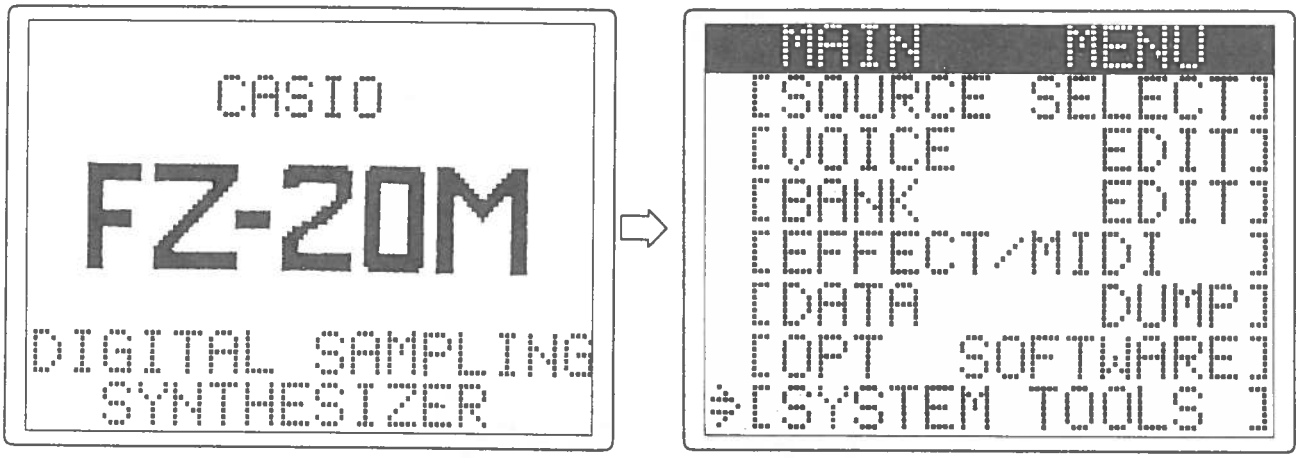
I BUILT-IN PROGRAM

1. BUILT-IN PROGRAM STARTING

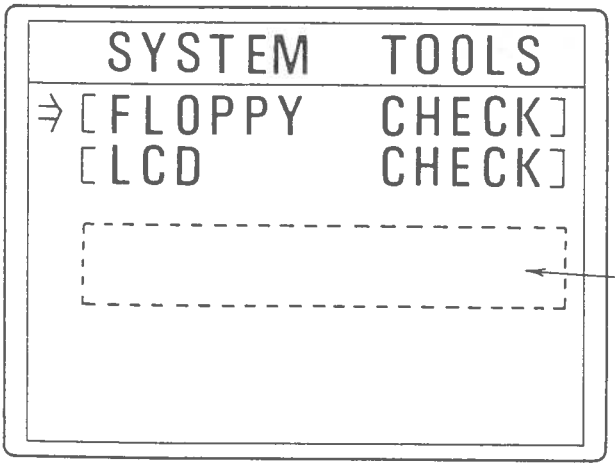
(1) Turn the power switch ON while pressing [DISPLAY] button.



(2) On the MAIN MENU, [SYSTEM TOOLS] is added.



(3) Moving down the cursor (⇒) by [▼] button, Select [SYSTEM TOOLS] then hit [ENTER] button.



(4) Now, either FDD Unit or LCD can be checked.

System ROM's version number will be shown here.

2. FDD UNIT CHECK

(1) Select [**FLOPPY CHECK**] in SYSTEM TOOLS menu then press [ENTER].

(2) Insert a floppy disc. (Do not use tone data disc or user's disc as the contents will be destroyed.)

(3) Select Read check or Write check by moving the cursor.

(4) Input logical value of checking sector, head, and track by ten key ([0] ~ [9]), [▲][▼] buttons, or VALUE slider.

☆ Conversion calculation of logical sector and actual sector, head, and track.

$$\begin{cases} \text{Sector} = (\text{Logical Sector})\ \%8 + 1 & (1 \sim 8) \\ \text{Head} = (\text{Logical Sector})\ \%16 \div 8 & (0 \sim 1) \\ \text{Track} = (\text{Logical Sector}) \div 16 & (0 \sim 79) \end{cases}$$

%8 means the reminder of Logical Sector/8.
(%8 of Logical Sector 100 is 4 as 100/8 is 12 (and) reminder 4.)

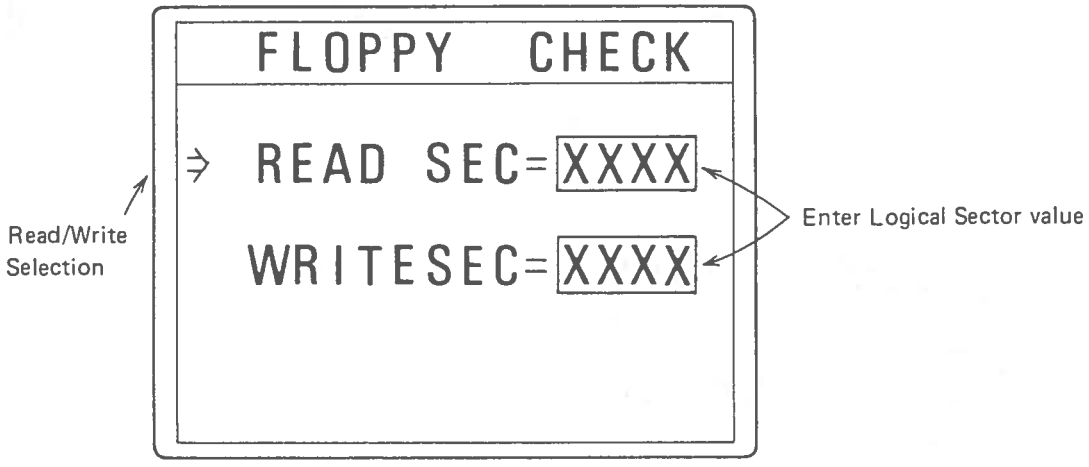
[Example] The last track and the last secor of the bottom side of adisc.

Sector : $\frac{1279}{8} = 159 + \frac{⑦}{8}$ Reminder ⟶ 7 + 1 = Sector 8

Head : $\frac{1279}{16} = 79 + \frac{⑮}{16}$ Reminder 15 ÷ 8 = 1.875 ⟶ Head 1 (bottom side)

Track : $\frac{1279}{16} = 79.9375$ ⟶ Track 79

Logical Sector : 1279



(5) After entering Logical Sector value, press [ENTER] button.

If the FDD Unit or FDC is mulfunction, the LCD indicates the following messages.

DATA ERROR	:	FDC is functioning but data has been changed.
FDC READ ERROR	:	FDC does not perform read operation properly.
FDC WRITE ERROR	:	FDC does not perform write operation properly.
DISC ERROR	:	FDD Unit does not output READY signal.

When FDC and FDD Unit function properly, the above messages will not be shown.

(6) Conversion Table of Logical Sector Value and Actual Sector, Track, Head

		Side 0 (Top)								Side 1 (Bottom)							
		0			Sector				8	0			Sector				8
0	Logical Sector	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
	Sector	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
	Head	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Track	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Logical Sector	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0039	0031
	Sector	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
	Head	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Track	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Logical Sector	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
	Sector	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
	Head	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Track	Track	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	Logical Sector	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
	Sector	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
	Head	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Track	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
	Logical Sector	0640	0641	0642	0643	0644	0645	0646	0647	0648	0649	0650	0651	0652	0653	0654	0655
	Sector	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
	Head	2	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Track	40	40	40	40	40	40	40	40	40	40	40	40	40	40	40	40
	Logical Sector	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
	Sector	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
79	Head	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
↓	Track	79	79	79	79	79	79	79	79	79	79	79	79	79	79	79	79

(7) FDD Unit's head can be cleaned by the following method..

a. Insert a cleaning sheet.
b. Enter Logical Sector Value "0000" then press [ENTER].
c. Enter Logical Sector Value "1271" then press [ENTER].
   The head 0 moves to the most inner position.
d. Repeat the above procedure a few times.
e. Head 1 (Bottom side) is cleaned by entering Logical Sector Values "0008" and "1279" a few times.

(8) Press [ESCAPE] button continuously for escaping from this check mode.

3. FDD UNIT ADJUSTMENT

(1) Insert an alignment disc.

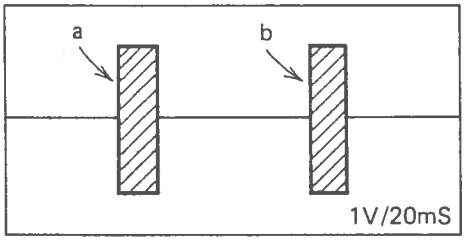
(2) Set Logical Sector Value of 0640 (for side 0) or 0648 (for side 1) in "READ SEC" of FLOPPY CHECK Menu.

(3) Perform Cat's Eye, Burst adjustments, and Azimuth confirmation.

Oscilloscope settings

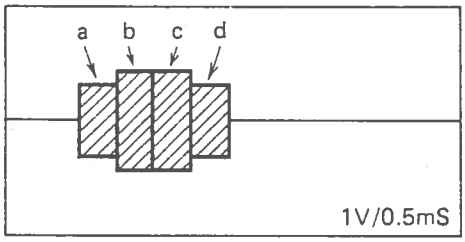
	RANGE	Trigger	Checkpoints
Channel 1	AC	+ or ⌐¬	Check pin T1
Channel 2	AC	- or ⌐¬	Check pin T2
External Channel	DC	+ or ⌐¬	Check pin INDEX

Cat's eye waveform
Sweep Time: 20mS
*Height of waves a and b should be same.



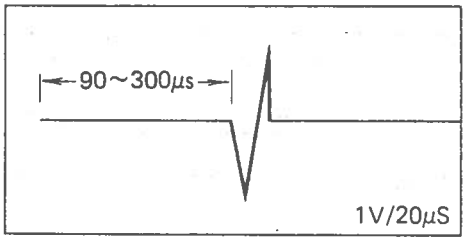
Cat's eye wave of "EPSON" alignment disc is square wave.

Azimuth waveform
Sweep Time: 0.5mS
*Confirm that height of a or d is lower than b or c.



- While reading an alignment disc, the LCD indicates "FDC ERROR".
- After the alignments, perform the same procedures after seeking the head from track 0 to track 40, and from track 79 to track 40.

Burst waveform
Sweep Time: 20μS



(4) Zero Track Alignment

Oscilloscope settings

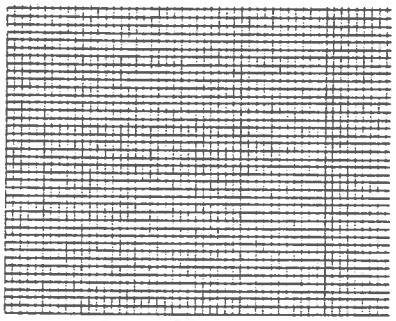
Channel	Range	Check points
Channel 1	DC	Check pin ZP
Channel 2	—	Not used
External Channel	DC	Check pin SP

Logical Sector Value	Voltage Level of Oscilloscope Screen
0000	HIGH
0016	HIGH
0032	LOW

4. LCD UNIT CHECK

(1) Select [**LCD CHECK**] in SYSTEM TOOLS Menu then press ENTER button.

(2) The LCD indicates all the dots.
Make sure that there is no missing dot.



(3) By pressing any one of the buttons, the LCD indicates the following characters.

■	⌟	□	×	÷	√	←	→	↑	↓	∞	ↄ	≠	≒	≤	≥
x	y	x̄	ȳ	x̂	ŷ	Δ	π	Σ	Ω	Γ	ʃ	³	−	¯	_
	!	″	#	$	%	&	′	(	)	*	+	,	−	.	/
0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
P	Q	R	S	T	U	V	W	X	Y	Z	[	¥	]	^	_
`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
p	q	r	s	t	u	v	w	x	y	z	{	|	}	~	

Confirm that all the characters are shown properly.

(4) The program finishes by hitting ESCAPE button.

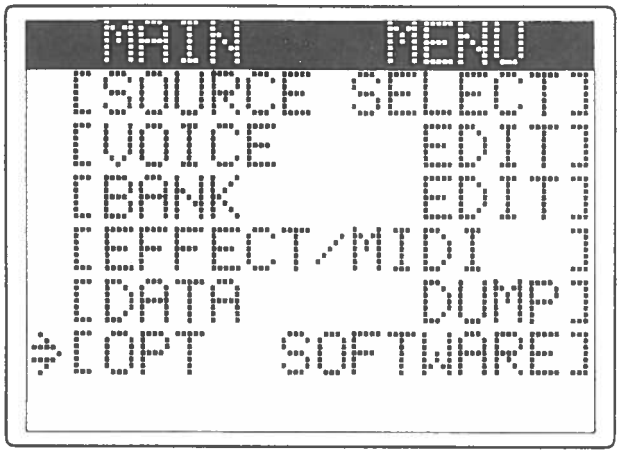
II DIAGNOSTIC FLOPPY DISC

1. STARTING OF DIAGNOSTIC PROGRAM

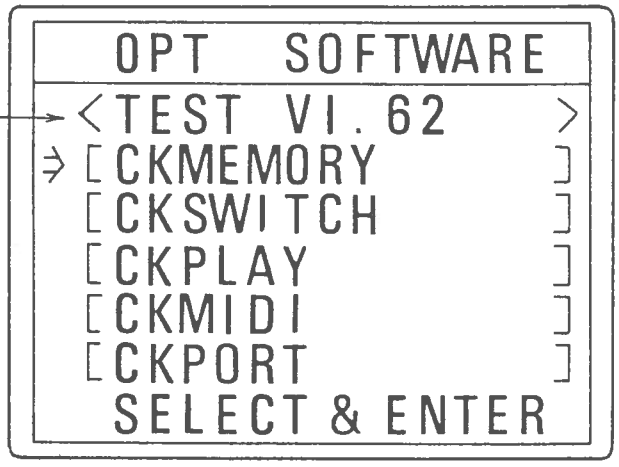
(1) Turn the power switch on.

(2) Insert the diagnostic disc.

(3) In the Main Menu, select [**OPT SOFTWARE**] then press [ENTER].



(4) The LCD indicates OPT SOFTWARE Menu.

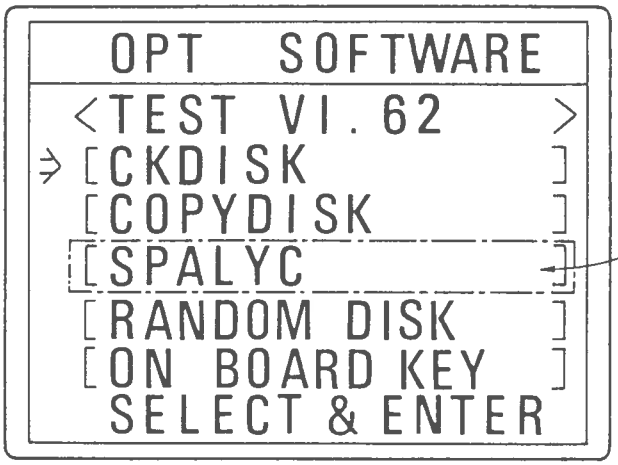


Page 1

Version number of the diagnostic disc.

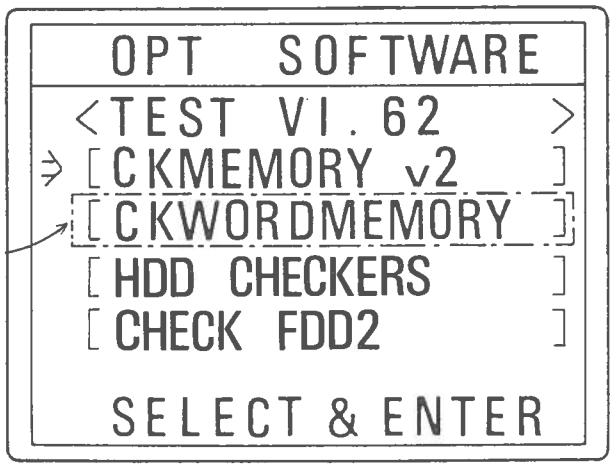
Check items can be selected by moving cursor by [▼] button then press [ENTER] button.

(5) Further pressing [▼] button from [**CKPORT**], the LCD shows the next page of OPT SOFTWARE Menu.



Page 2

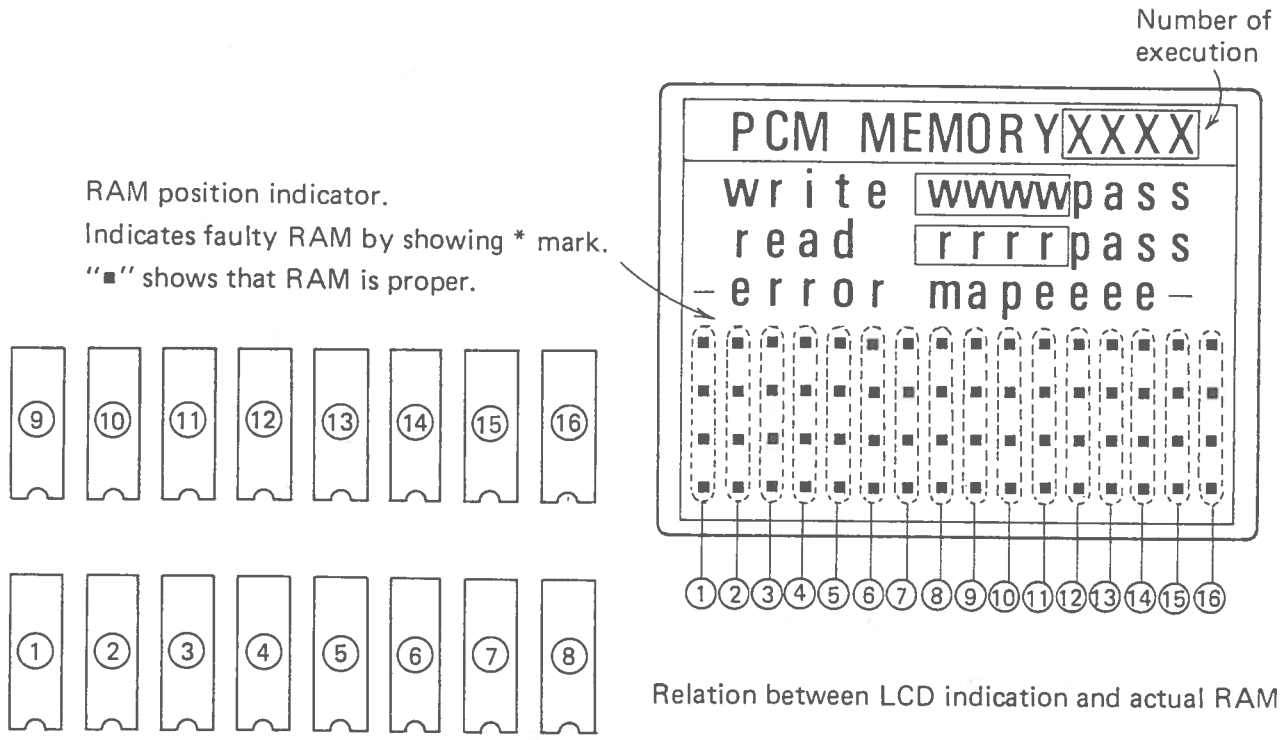
cannot be used.



Page 3

2. WAVE MEMORY RAM CHECK (1)

(1) Select [**CKMEMORY**] in OPT SOFTWARE Menu then press [ENTER] button.



Relation between LCD indication and actual RAMs.

Number in "wwww" counts up while writing data in the RAMs.

Number in "rrrr" counts up while reading data from the RAMs.

Reading and writing data is done by every 127K byte as shown below.

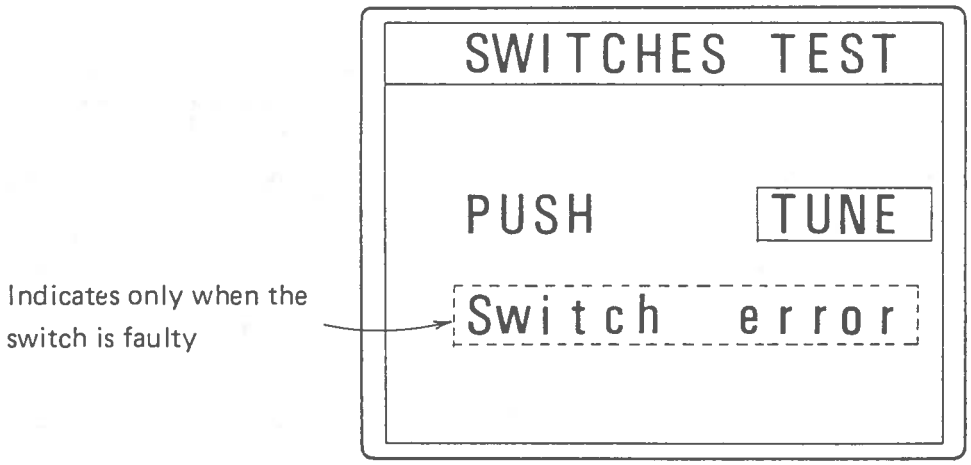
→127→255→383→511→639→767→895→1023→1151→1279→1407→1535→1663→1791→1919→2047

*When all the RAMs function properly, "eeee" in error map shows 0000 and all the RAM indicators are dots.
If one of the RAMs is faulty, the faulty address is shown in "eeee" and RAM position indicator displays the faulty RAM by * mark.

(2) Hitting of any button finishes the check program.

3. SWITCH CHECK

(1) Select **[CKSWITCH]** in OPT SOFTWARE Menu.



(2) Press all the buttons in order as indicated in the LCD.

(3) After checking of all the switches, connect a pedal switch and press it.

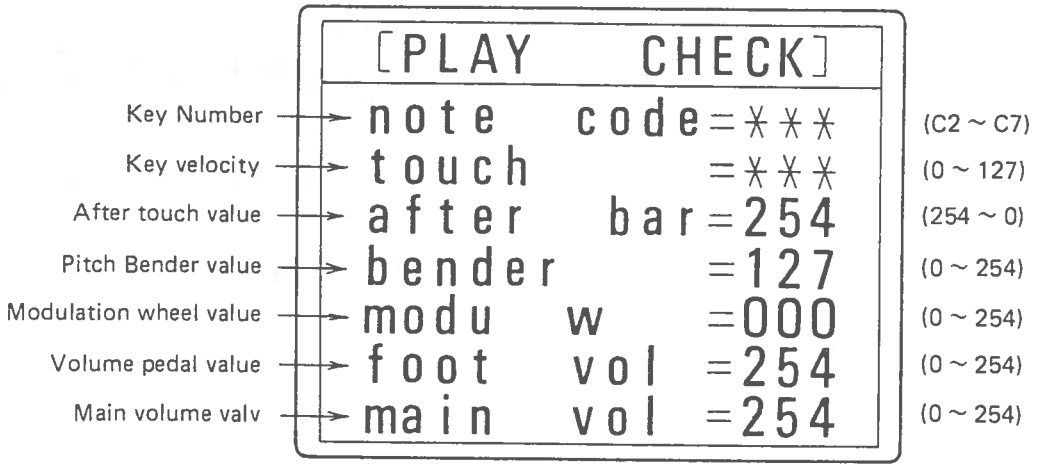
(4) If all the switches function properly, the LCD indicates "All switch OK".

(5) The FZ-20M can be escaped from the program by pressing ESCAPE button after all the switch checking is completed.
The program cannot be released if the checking is not completed.

4. KEYS, SENSORS, AND VR CHECK

(1) Connect the FZ-20M with a MIDI keyboard.

(2) Select [**CK PLAY**] in OPT SOFTWARE Menu then press ENTER.



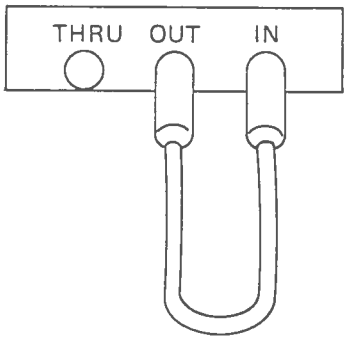
(3) Hitting keys and moving controls on the MIDI keyboard vary the corresponding value on the LCD.

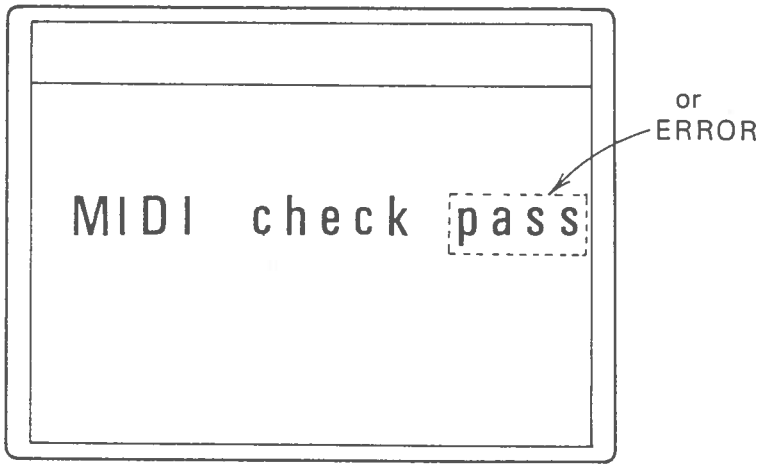
* If the connected keyboard does not have MIDI transmit function, the LCD value of the corresponding control will not change.

(4) ESCAPE button finishes the program.

5. MIDI CHECK

(1) Connect MIDI IN and OUT terminals of the FZ-20M by a MIDI cable.





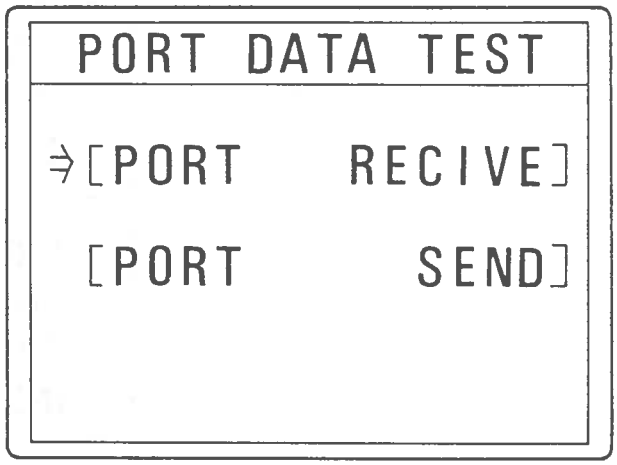
(2) Select [**CK MIDI**] in OPT SOFTWARE Menu then press ENTER.

(3) When the MIDI circuits are normal, the LCD indicates "MIDI check pass".
"MIDI check error" will be shown on the LCD if the MIDI circuit is faulty.

6. EXTERNAL PORT CHECK

(1) Connect a properly functioning FZ-10M/20M or FZ-1 and the FZ-20M which should be checked with a EXTERNAL PORT cable.

(2) Select **[CK PORT]** in OPT SOFTWARE Menu and press ENTER button.



(3) Select **[PORT RECEIVE]** on the test unit (The FZ-20M that should be checked) then press ENTER.
Assign **[PORT SEND]** on the other FZ-1 or FZ-10M/20M then hit ENTER.

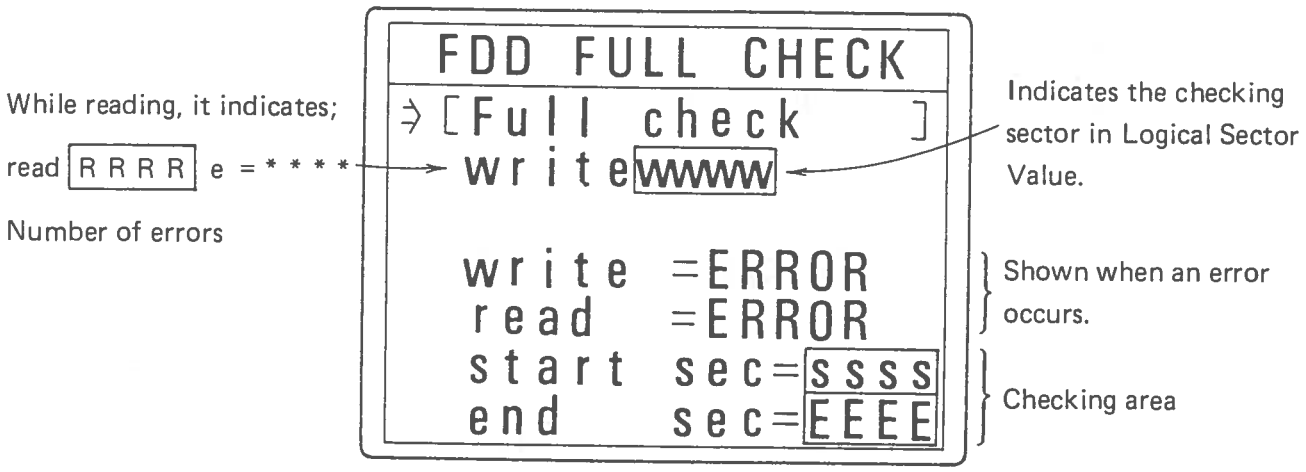
(4) The test unit indicates "executed OK" when External Circuit functions properly.
"PORT ERROR" or "TIME OUT" will be shown when External Circuit is malfunction.

(5) Perform the same test by setting [PORT SEND] on the test unit and **[PORT RECEIVE]** on the other FZ-1 or FZ-10M.

7. FDD READ/WRITE AGING TEST

(1) Select [**CK DISC**] in OPT SOFTWARE Menu and hit [ENTER] button.

(2) Insert an empty floppy disc.



(3) Moving the cursor at "start sec" by [▼] button, then enter the starting sector in Logical Sector Value.

(4) Set the Logical Sector Value of end sector after selecting "end sec".

(5) Move the cursor to [**Full check**] by [▲] button then press [ENTER].

(6) FDD Unit then repeats writing and reading data in the selected checking area and indicates "write = ERROR" or "read = ERROR" if an error occurs.

(7) If an error occurs, perform the followings.

a. Head cleaning
b. Replace the disc if errors always occur in the same sector.
c. FDD Unit alignment (Cat's eye, Burst alignments)

8. DISK COPY

(1) Select [**COPYDISK**] then press [ENTER] button.

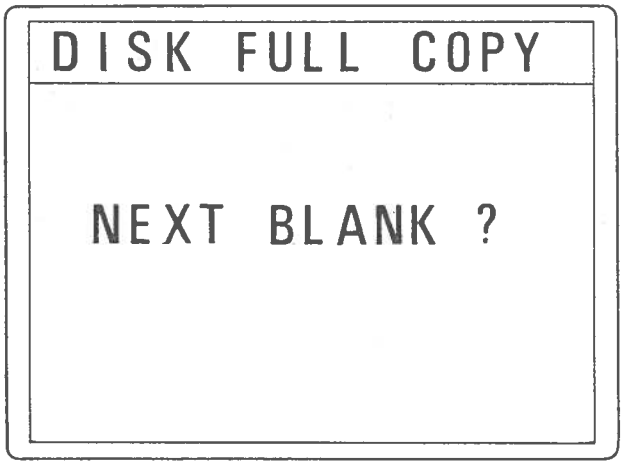
(2) Display indicates **"INSERT MASTER"**.

(3) Insert the master disk then press [YES] button.

(4) While the FZ-20M is reading the master disk, it indicates **"READING MASTER"** on the LCD.

(5) When the LCD indicates **"INSERT BLANK"**, set a blank disk and press [YES] button.

(6) If the disk is copied, the LCD indicates;



Press [YES] and repeat the above (2) to (5) if more copy is required.

Pressing [NO] escapes the program to the main menu.

9. RANDOM DISK CHECK

(1) Select [**RANDOM DISK**] then press [ENTER].

(2) By pressing [ENTER], the FDD reads random sectors.

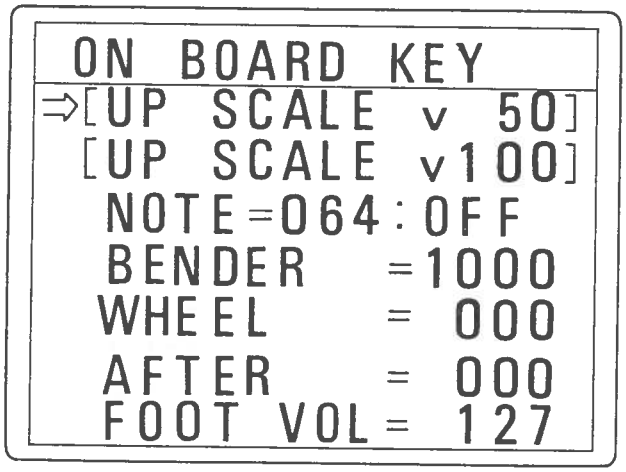
(3) Pressing [ESCAPE] twice returns the FZ-20M to the main menu.

10. ON BOARD KEY

(1) Load a sound disk in the FZ-20M.

(2) Insert diagnostic disk and choose [**ON BOARD KEY**] in OPT SOFTWARE menu then press [ENTER] button.

(3) The display indicates;



(4) By selecting [**UP SCALE v50**] and [ENTER] button, the FZ-20M outputs C1 ~ C6 notes sounds with velocity value 50.

(5) [**UP SCALE v100**] does the same with velocity value 100.

(6) If **NOTE = 64** column is choosen, buttons [1] to [8] provides C2 ~ C3 notes sound. By [YES] button, 7-note polyphonic sound will be output one by one.

(7) On the above sounds, effect value can be added by changing **"BENDER", "WHEEL", "AFTER", "FOOT VOL"** values on the display.

11. WAVE MEMORY RAM CHECK (2)

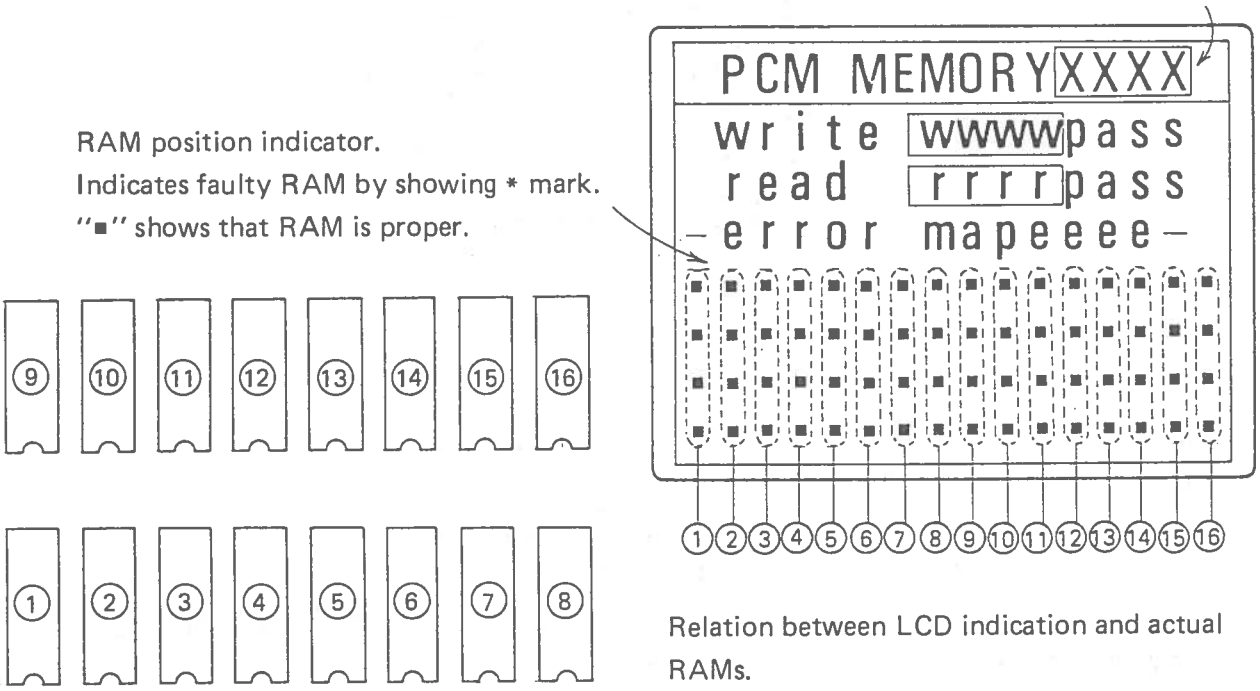
This program checks Wave Memory RAMs more severely than **WAVE MEMORY RAM CHECK (1)** on page 18 by writing and reading data in the RAMs while all the FZ-20M circuits are fully operated.

If no error occurs after four execution cycles of writing and reading, all the dynamic RAMs can be considered as proper.

The display may show proper RAM as faulty if the program is performed more than 5 execution cycles.

All the RAMs are good if this block indicates 0005

RAM position indicator.
Indicates faulty RAM by showing * mark.
"■" shows that RAM is proper.



Relation between LCD indication and actual RAMs.

The operation method is same as it of **WAVE MEMORY RAM CHECK (1)** on page 18 except selecting **[CKMEMORY v2]** in OPT SOFTWARE menu.

12. HARD DISK CHECK

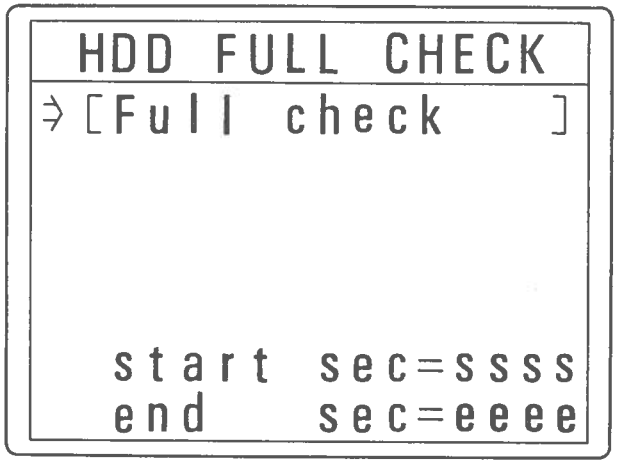
Note that all the data in the hard disk will be eliminated after the following procedures.

(1) Connect proper hard disk

(2) Turn the hard disk and FZ-20M on

(3) Insert diagnostic disk and choose [HDD CHECKERS] in OPT SOFTWARE menu then press [ENTER] button.

(4) LCD display indicates;

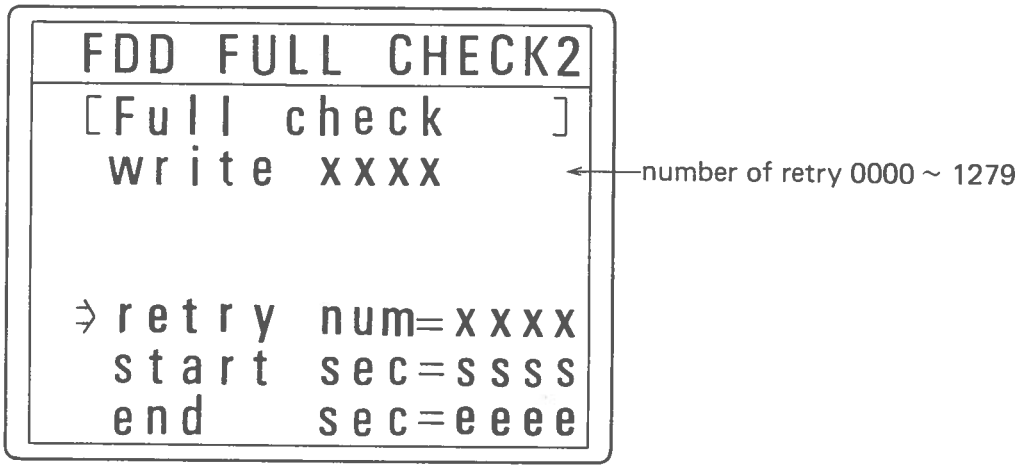


(5) Moving the cursor at "start sec" by [▼] button, then enter the starting sector number by ten-key or VALUE slider.

(6) Move the cursor on [Full check] and press [ENTER].
FZ-20M will perform write/read check within the designated area in the hard disk, and shows so if an error occurs.

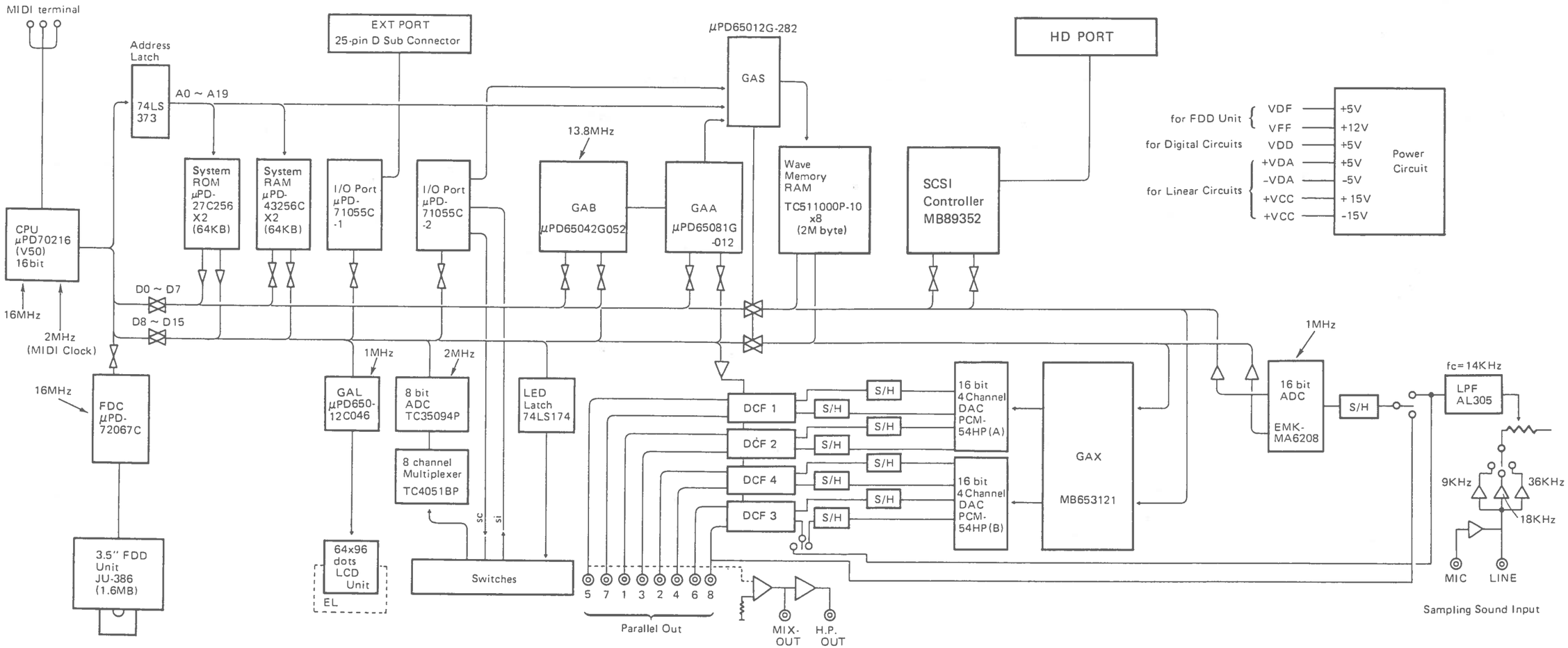
13. FDD FULL CHECK 2

The FZ-20M will check the designated area of the floppy disk until error rate agrees with the set number of retry.
Refer to page 20 for the operation.



CIRCUIT EXPLANATION

BLOCK DIAGRAM



CPU μPD70216 is a 16-bit microprocessor and controls all the devices.
System ROMs contain the FZ-10M's system program whereas System RAMs are for the work area of the program.

Recorded sound's waveform is transformed in 16-bit x 1024K steps digital data by a 16-bit ADC (Analog to Digital Converter) EMK-MA6208 and stored in Wave Memory of 16 pieces of 1024K-bit dynamic RAMs.
The gate arrays GAA and GAB are for accessing of Wave Memory RAMs.
When Playbacking, data from Wave Memory pass through gate array GAX which controls the Cross Fading.

The outputs of GAX are transformed in analog waveforms by two DACs PCM-54HP (A) and (B). By means of time sharing, S/H (Sample and Hold) circuits separate the eight DAC outputs one by one and send them to DCFs which is a digital controlled filter and gain controller.

TC35094P converts analog inputs from master volume control and value slider into digital data.
Gate array GAL is a interface between CPU and 64 x 96 dots graphic LCD Unit.

μPD71055Cs are I/O Ports and performs switch scanning, upper address designation of Wave Memory RAMs, and interface between the CPU and External device.
μPD72067C controls the FDD (Floppy Disc Drive) JU-255.

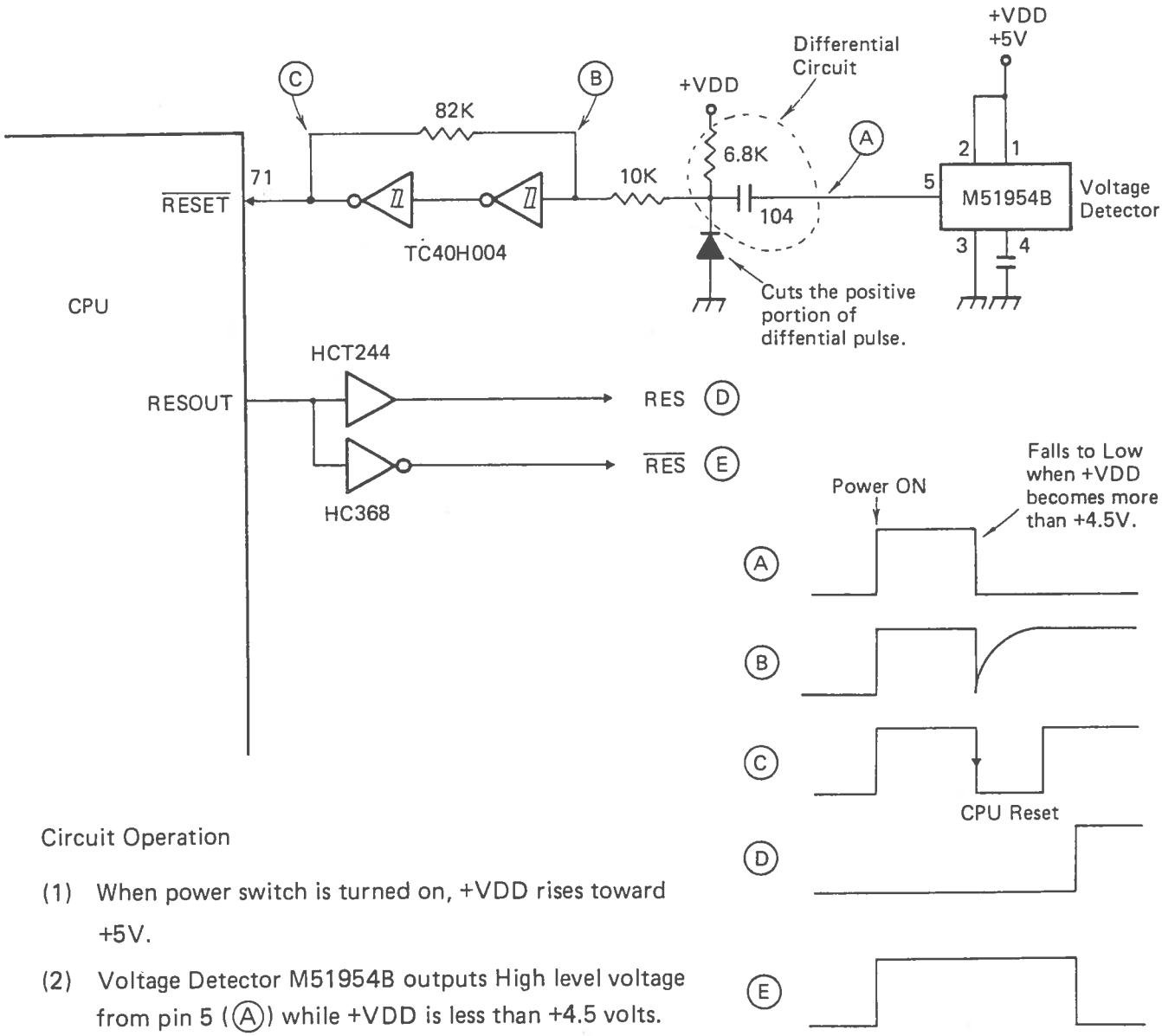
CPU data is converted in HD (Hard disk) signal by MB89352

CPU (μPD70216)

μPD70216 is a 16-bit C-MOS LSI and controls all the peripheral devices.
The following is pin functions of the CPU.

Pin No.	Terminal	In/Out	Function
78~80, 1	A19 (PS3) ~ A16 (PS0)	Out	Upper address bus
3 ~ 10	AD15 (A15)~AD8 (A8)	In/Out	Upper address or data bus
13	GND	–	Ground (0V) source
14 ~ 21	AD7 ~ AD0	In/Out	Lower address or data bus
27	$\overline{\text{DMARQ1}}$	IN	Data request from SCSI Controller
28	$\overline{\text{DMAACK0}}$	OUT	Acknoledge signal to SCSI Controller
31	DMARQ3 (RXD)	In	MIDI data input
32	DMAAK3 (TXD)	Out	MIDI data output
35	VDD	–	VDD (+5V) source
37	INT2	In	Interrupt from gate array GAB
40	INT5	In	Interrupt from I/O Port 1
44	TCLK	In	2MHz clock pulse for built-in timer
45	TOUT2	Out	Built-in timer output
50	ASTB	Out	Address latch enable signal. When High, signal AD0 ~ AD15 becomes address bus.
51	$\overline{\text{UBE}}$	Out	A part of System RAM2 chip select signals.
52, 54	GND	–	Ground (0V) source
55, 56	X2, X1	In	16MHz clock pulse inputs
57	CLK OUT	Out	8MHz (a half of 16MHz) clock pulse for gate array GAS
58	$\overline{\text{BUF EN}}$	Out	Data bus buffer enable signal. When Low, Bidirectional Bus Buffers LS245's become functional.
59	BUF R/W	Out	Data bus read/write signal. When High, data is transferred from CPU to other devises whereas the data transfer direction is from devices to CPU when this terminal is Low.
61	$\overline{\text{IO WR}}$	Out	I/O devices write signal. When Low, CPU is able to write data in the I/O devices.
62	$\overline{\text{M WR}}$	Out	Memory devices write signal. When Low, CPU is able to write data in the memory devices.
64	$\overline{\text{IO RD}}$	Out	I/O devices read signal. When Low, CPU is able to read data from the I/O devices.
65	$\overline{\text{M RD}}$	Out	Memory device read signal. When Low, CPU is able to read data from the memory devices.
70	READY	In	Receiving High level signal from this terminal, CPU acknowledges that gate array GAS is not busy.
71	$\overline{\text{RESET}}$	In	At Power ON, the terminal receives a Low level pulse which resets the CPU.
72	VDD	–	+5V source
74	RES OUT	Out	Power ON reset signal for I/O devices
77	$\overline{\text{REF RQ}}$	Out	Refresh request signal. Falls to Low level when CPU requests Dynamic RAMs to reflesh.

CPU RESET CIRCUIT



Circuit Operation

(1) When power switch is turned on, +VDD rises toward +5V.

(2) Voltage Detector M51954B outputs High level voltage from pin 5 (Ⓐ) while +VDD is less than +4.5 volts.

(3) When +VDD becomes higher than +4.5 volts, pin 5 of M51954B (Ⓐ) falls to Low.

(4) At the falling edge of pin 5, a differential pulse is generated in the differential circuit (Ⓑ).

(5) The differential pulse is shaped in a square pulse by the two inverters (Ⓒ).

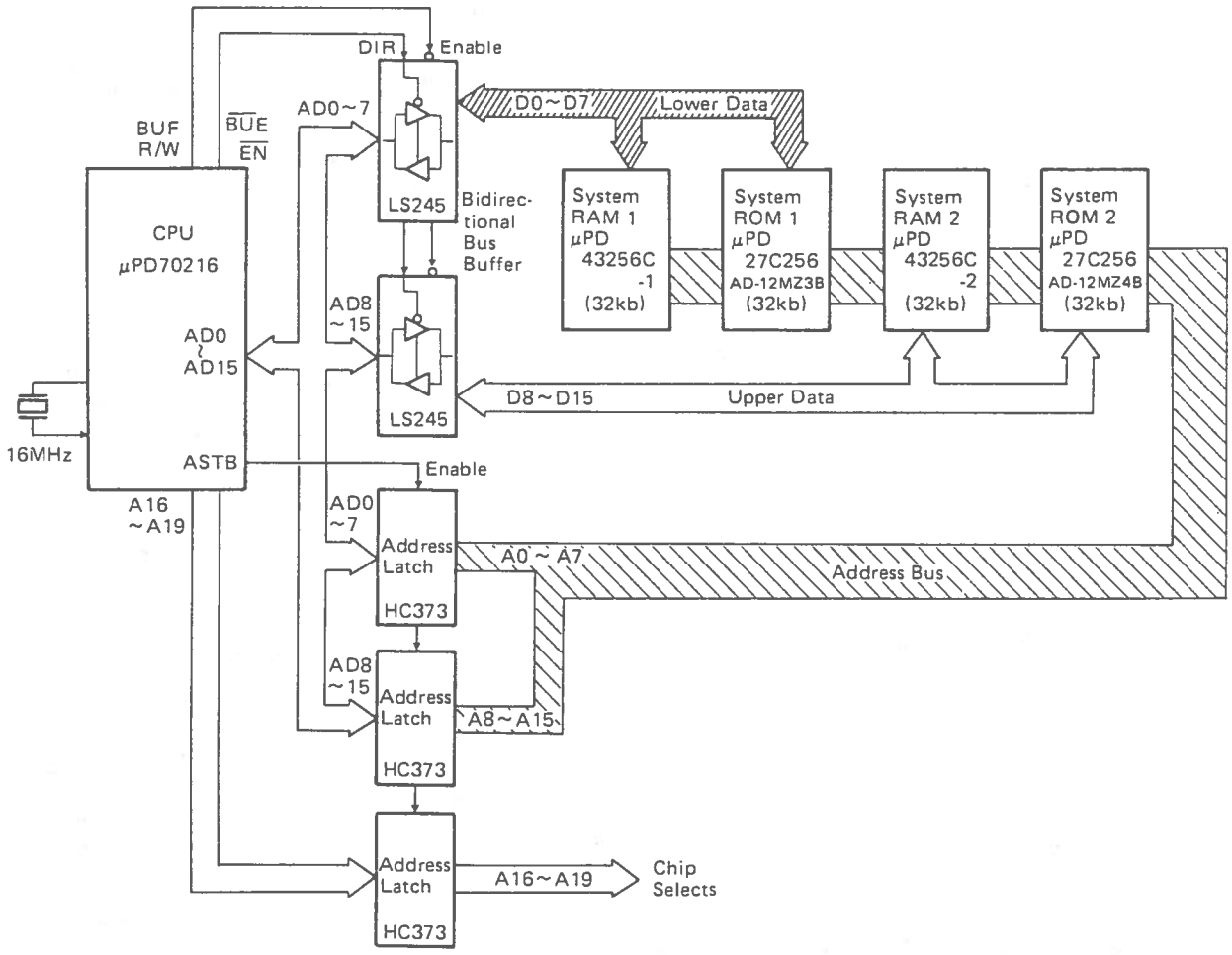
(6) CPU initialize the internal circuits at the falling edge of Reset signal (Ⓒ).

(7) After the initialization of the internal circuits, CPU resets all the devices by signal RES OUT (Ⓓ and Ⓔ).

SYSTEM ROM/RAM

1. System ROM/RAM Access

System ROMs contain the FZ-20M's system program whereas System RAMs are for the work area of the program.



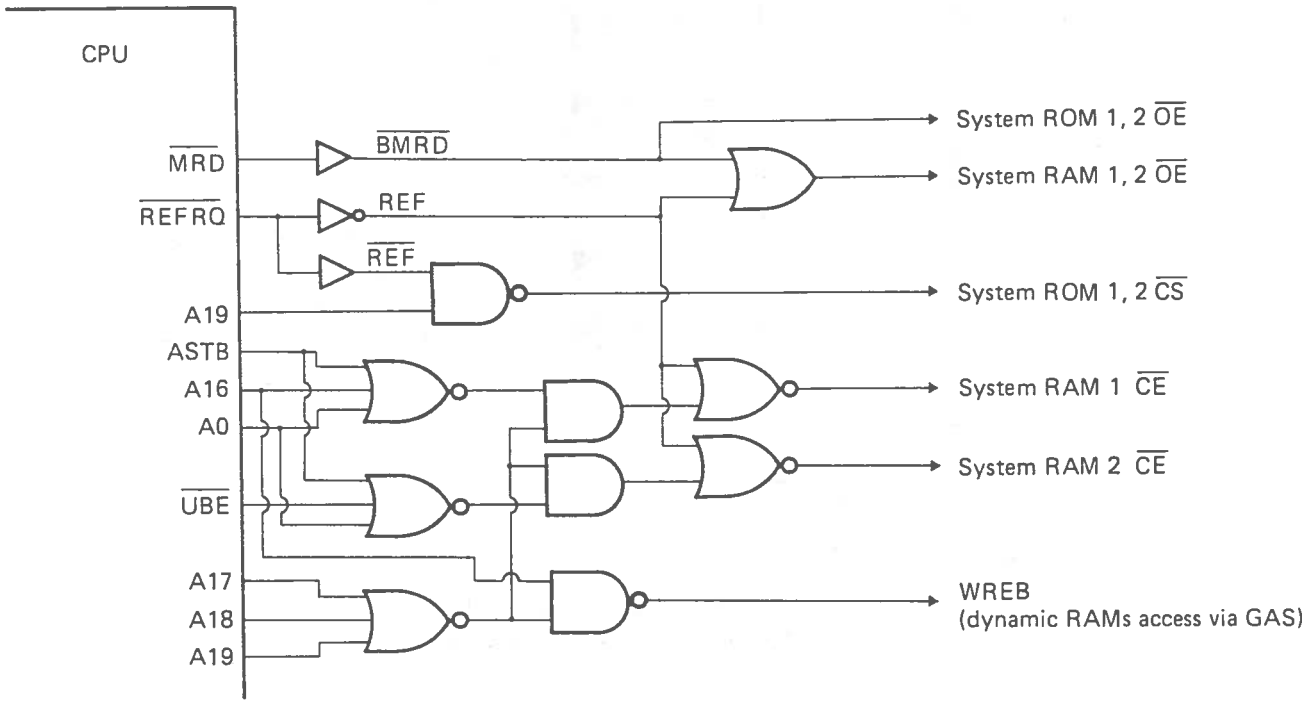
Signals AD0 ~ AD15 function as either data bus or address bus.
When the bus carries an address, CPU raises signal ASTB so that Address Latches (HC373s) are able to take the signals in and send them to the address terminals of the ROMs and the RAMs.

LS245 is a bidirectional buffer which determines the direction of data flow by signal BUF R/W of the CPU.

Signal BUF R/W	Data Flow
High	CPU ← - - - - ROM/RAM
Low	CPU - - - - → ROM/RAM

Since the data bus is 16-bit and data terminals of the ROMs and RAMs are 8-bit, the data is divided in half and stored in each ROM or RAM separately.

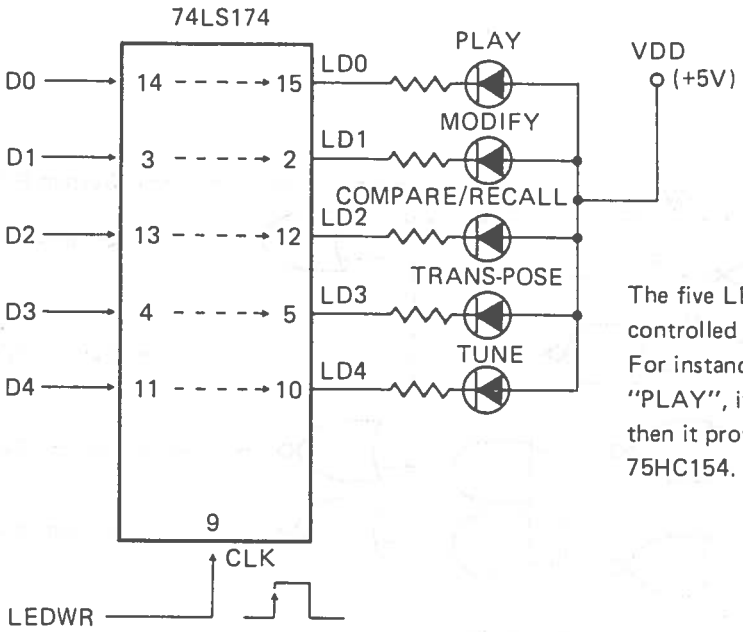
2. System ROM/RAM Chip Selection



System ROMs and RAMs are designated when both $\overline{OE}$ and $\overline{CE}$ terminals are Low level. When CPU falls $\overline{MRD}$ terminal, $\overline{CE}$ of System ROM 1, 2 and $\overline{OE}$ and $\overline{CE}$ of System RAM 1, 2 falls Low level selecting the System RAMs. At this time, if signal A19 rises to High, $\overline{CS}$ of System ROM 1, 2 become Low level and the ROMs are selected.

While CPU is generating refresh signals for the dynamic RAMs (Wave Memory RAMs), signal $\overline{REF\ RQ}$ falls to Low level raising $\overline{OE}$ and $\overline{CE}$ of System RAMs so that System RAM 1 and 2 cannot be designated.

LED LATCH (74LS174)

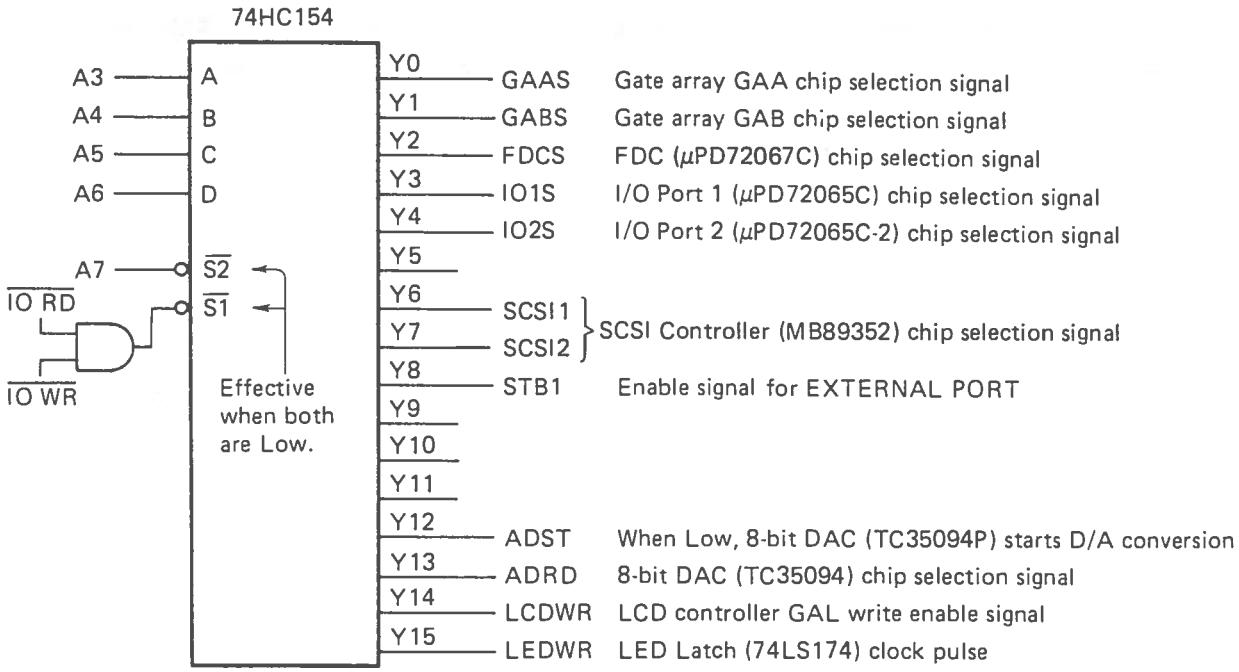


The five LEDs on the operation panel is controlled by LED Latch.
For instance, when CPU lights LED "PLAY", it drops signal D0 of data bus then it provides signal LED WR via 75HC154.

The contents of data bus D0 ~ D4 is latched and kept until 74LS174 receives next CLK pulse.

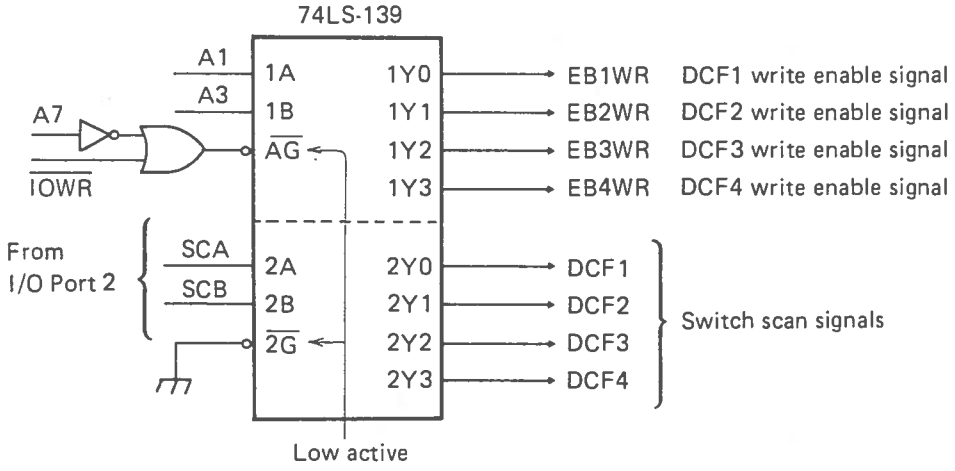
CHIP SELECTOR

By the combinations of signals A3 ~ A6, one of the outputs falls to Low level and becomes a chip selection signal.



DECODER (74LS139)

By the combination of signals A1, A3, SCA, and SCB, Decoder outputs write enable signal of the DCFs and switch scan signals.

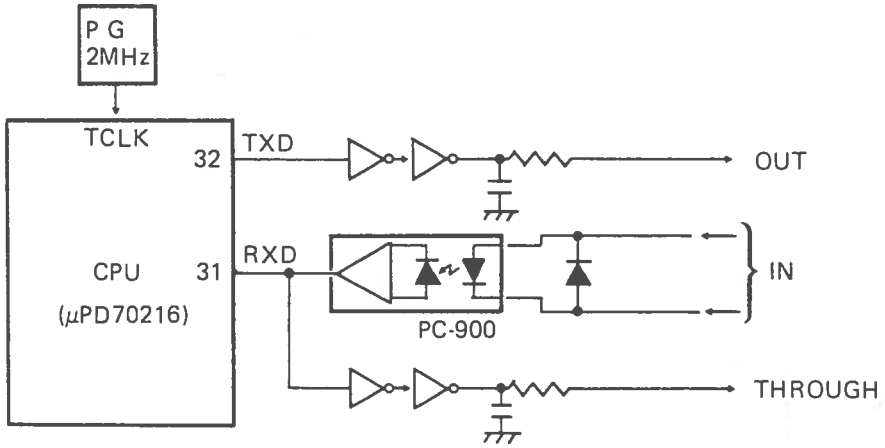


Switch Matrix

	SI0	SI1	SI2	SI3	SI4	SI5	SI6	SI7
SC0	0	1	2	3	4	5	6	7
SC1	8	9	YES	NO				
SC2	UP	DOWN	RIGHT	LEFT	ENTER	ESCAPE	DISPLAY	
SC3	PLAY	MODIFY	COMPARE /RECALL	TRANS- POSE	TUNE			

To I/O Port 2

MIDI CIRCUITS



I/O PORT 1 (μPD71055-1)

I/O Port 1 controls External Port, FDC (Floppy Disc Controller), gate arrays GAA and GAB.

Pin No.	Terminal	Signal	In/Out	Function
1	PO3	IF3	In/Out	Data bus for External Port
2	PO2	IF2	In/Out	
3	PO1	IF1	In/Out	
4	PO0	IF0	In/Out	
5	$\overline{RD}$	$\overline{BIO\ RD}$	In	Read signal. CPU falls this terminal Low when it reads data from I/O Port 1
6	$\overline{CS}$	$\overline{IO1S}$	In	Chip select signal from CPU. I/O Port 1 is designated when this terminal is Low.
7	GND	GND	–	Ground (0V) source
8	A1	A2	In	Port selection signals. Voltage levels of these terminals select port 0 (P00~P07), port 1 (P10~P17), or port 2 (P20~P27).
9	A0	A1	In	
10	P27	OBF	Out	Control signals for External Port
11	P26	ACKE	In	
12	P25	IBF	Out	
13	P24	–	In	
14	P20	ACKO	Out	
15	P21	STBO	Out	
16	P22	IFOUT	Out	
17	P23	IF INT	Out	Interrupt signal to CPU when using External Port
18	P10	GAAR	In	Gate array GAA ready signal
19	P11	GABR	In	Gate array GAB ready signal
20	P12	LCR	In	Gate array GAL ready signal
21	P13	ADR	In	8-bit ADC (TC35094P) ready signal. Receives High level signal when A-D conversion is completed in TC35094P.
24	P16	IF IN	In	Control signal from External Port
25	P17	FD INT	In	Interrupt signal from DCF. When DCF require new data, this terminal receives High level signal.
26	VDD	VDD	–	VDD (+5V) source
27~34	D7 ~ D0	D7 ~ D0	In/Out	Data bus between CPU
35	RESET	RES	In	Power ON reset signal
36	$\overline{WR}$	$\overline{BIO\ WR}$	In	Falls to Low when CPU outputs data via this I/O Port
37	PO7	IF7	In/Out	Data bus for External Port
38	PO6	IF6	In/Out	
39	PO5	IF5	In/Out	
40	PO4	IF4	In/Out	

I/O PORT 2 (μPD71055-2)

I/O Port 2 performs switch scanning, gain control of sample sound, gate array GAS controlling and DCF controlling.

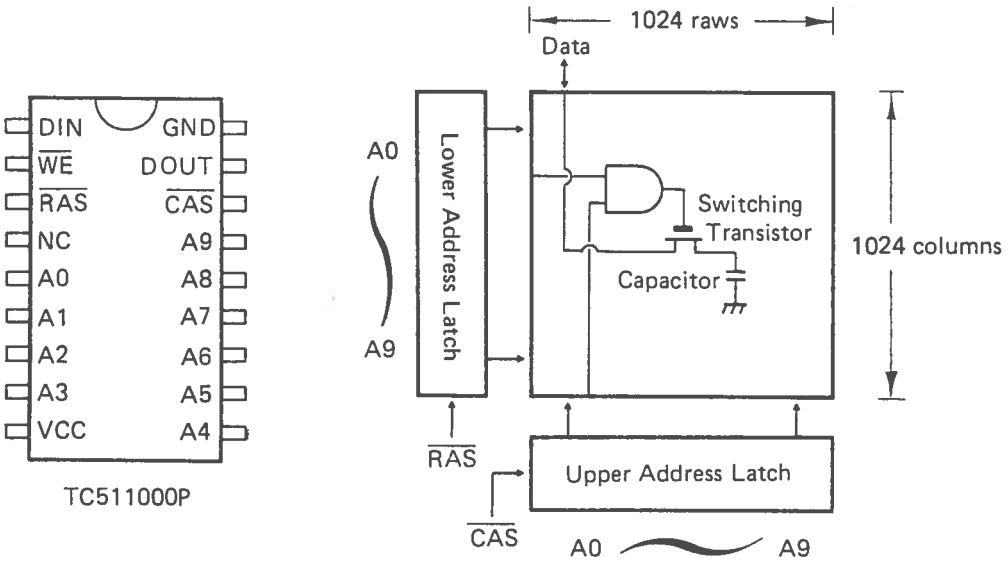
Pin No.	Terminal	Signal	In/Out	Function
40	PO4	ADS2	Out	8-bit ADC input selection signals. By the combinations of these signals, input of 8-bit ADC is selected.
1	PO3	ADS1	Out	
2	PO2	ADS0	Out	
3	PO1	SCB	Out	Switch scanning signals
4	PO0	SCA	Out	
5	$\overline{RD}$	$\overline{BIO\ RD}$	In	Read signal from CPU. CPU falls this terminal Low when it reads data from I/O Port 2.
6	$\overline{CS}$	IO2S	In	I/O Port 2 chip select signal.
7	GND	GND	–	Ground (0V) source
8	A1	A2	In	Port selection signals. Voltage levels of these terminals select port 0 (P00~P07), port 1 (P10~P17), or port 2 (P20~P27).
9	A0	A1	In	
10~17	P27 ~ P23	SI7~SI3	In	Switch input signals
18~23	P10 ~ P14	16B~20B	Out	Upper 5 bits of Wave Memory RAM address
24	P16	GAIN	Out	Sampling gain control Sample Gain: H → P16 Low; L → P16 High
25	P17	NORM	Out	Sampling frequency switching signal. Low level when sampling frequency is 36KHz and High when 18KHz or 9KHz.
26	VDD	VDD	–	VDD (+5V) source
27~34	D7 ~ D0	D7~D0	In/Out	Data bus between I/O Port 2 and CPU
35	RESET	RES	In	Power ON reset signal (High active)
36	$\overline{WR}$	$\overline{BIO\ WR}$	In	Write signal. CPU falls this terminal when it sends data via I/O Port 2.
37	PO7	INUSE	Out	Being Low, this signal selects the FDD Unit and lights the FDD BUSY lamp.
38	PO6	$\overline{MO\ ON}$	Out	FDD Unit's motor drive signal
39	PO5	TC	Out	High level when data transfer to FDC is completed

WAVE MEMORY RAM (TC511000P)

1. Dynamic RAM

Hitherto, static RAMs have been employed in Casiotone as memory devices.
Static RAMs use six transistors per one bit and turning these transistors on or off, digital signals of High or Low levels are stored.
Since stored data are kept as long as power sources are provided, controlling of static RAMs are made simple but, as the cost per one bit is rather high, static RAMs are unsuitable for a large memory area.

The FZ-20M employes dynamic RAM TC511000P whose capacity is 1 megabit for storing sample sound data.
Dynamic RAM contains capacitors which store digital data by being charged or discharged.
Since a capacitor does not hold the electric charge for a long time, the stored data must be rewritten periodically. This rewriting is called **refresh.** Also, due to reducing number of pin terminals, addressing is made twice for raws and columns.
As the access of a dynamic RAM is thus complicated, the control circuits become intricate.



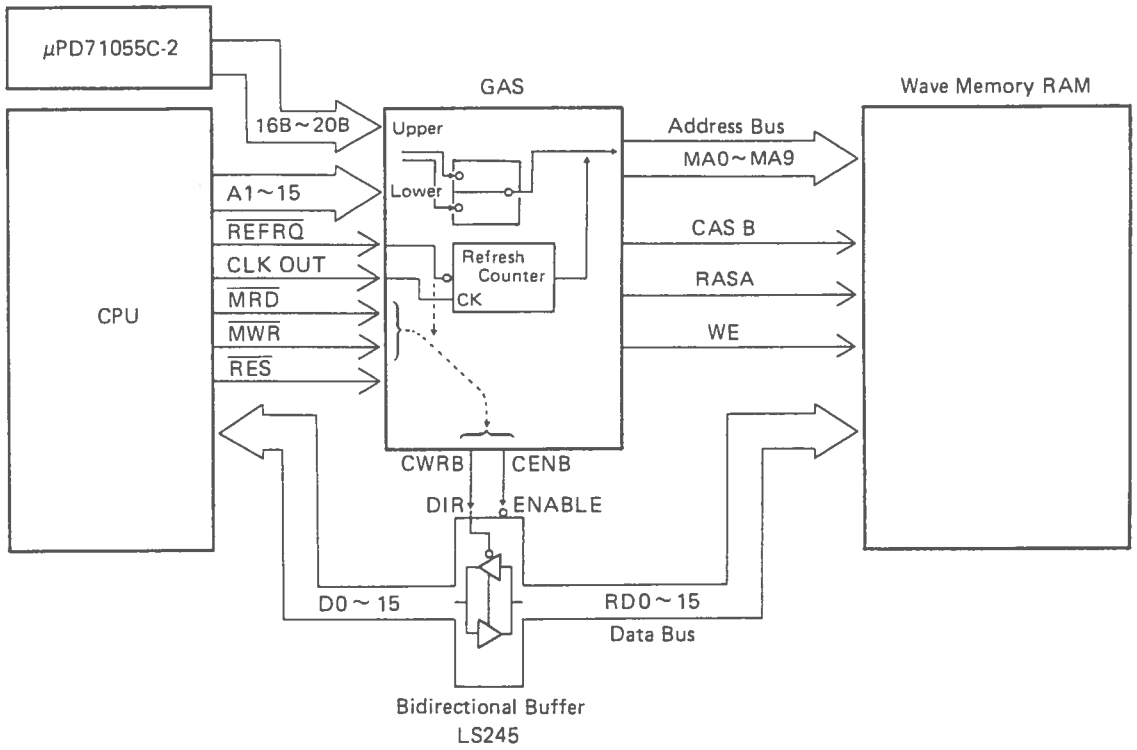
Addressing is made by selecting a column (upper address) first, then a row (lower address).
The address signals A0 ~ A9 are put into the upper or lower address latches when enable signals $\overline{CAS}$ (Column Address Strobe) or $\overline{RAS}$ (Row Address Strobe) fall to Low level.

Since dynamic RAMs do not have CE (Chip Enable) or OE (Out Enable) terminals, chip selection is made when $\overline{RAS}$ terminal falls and stored data emerges while $\overline{CAS}$ is Low.

Via a refresh counter in gate array GAS, CPU designates all the addresses periodically for re-charging the capacitors in dynamic RAM.

2. Wave Memory RAM Access

Wave Memory RAMs are controlled by CPU via gate array GAS.



Address bus A1 ~ A15 from CPU and 16B ~ 20B from I/O Port 2 are separated in upper and lower addresses in gate array GAS. The upper and lower addresses are provided alternately from MA0~ MA9 terminals of GAS.

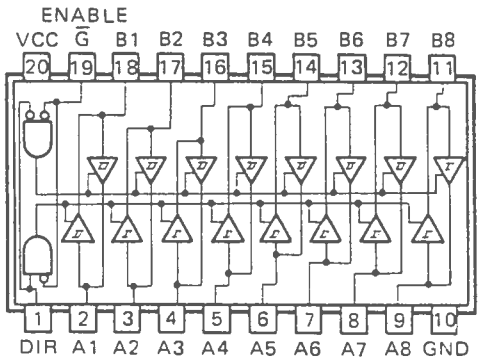
Wave Memory RAMs descriminate MA0 ~ MA9 as upper or lower addresses by signal RAS A or CAS which are generated in GAS.

In order to recharge the memory cell capacitors of Wave Memory RAMs, CPU periodically send signal $\overline{\text{REF RQ}}$ to GAS.

By $\overline{\text{REF RQ}}$ and 8MHz clock pulse of CLK OUT, refresh counter in GAS starts counting and designates all the addresses of Wave Memory RAMs in turn.

The direction of data flow between CPU and Wave Memory RAMs is controlled by signal $\overline{\text{MRD}}$ and $\overline{\text{MWR}}$ and the bidirectional buffer.

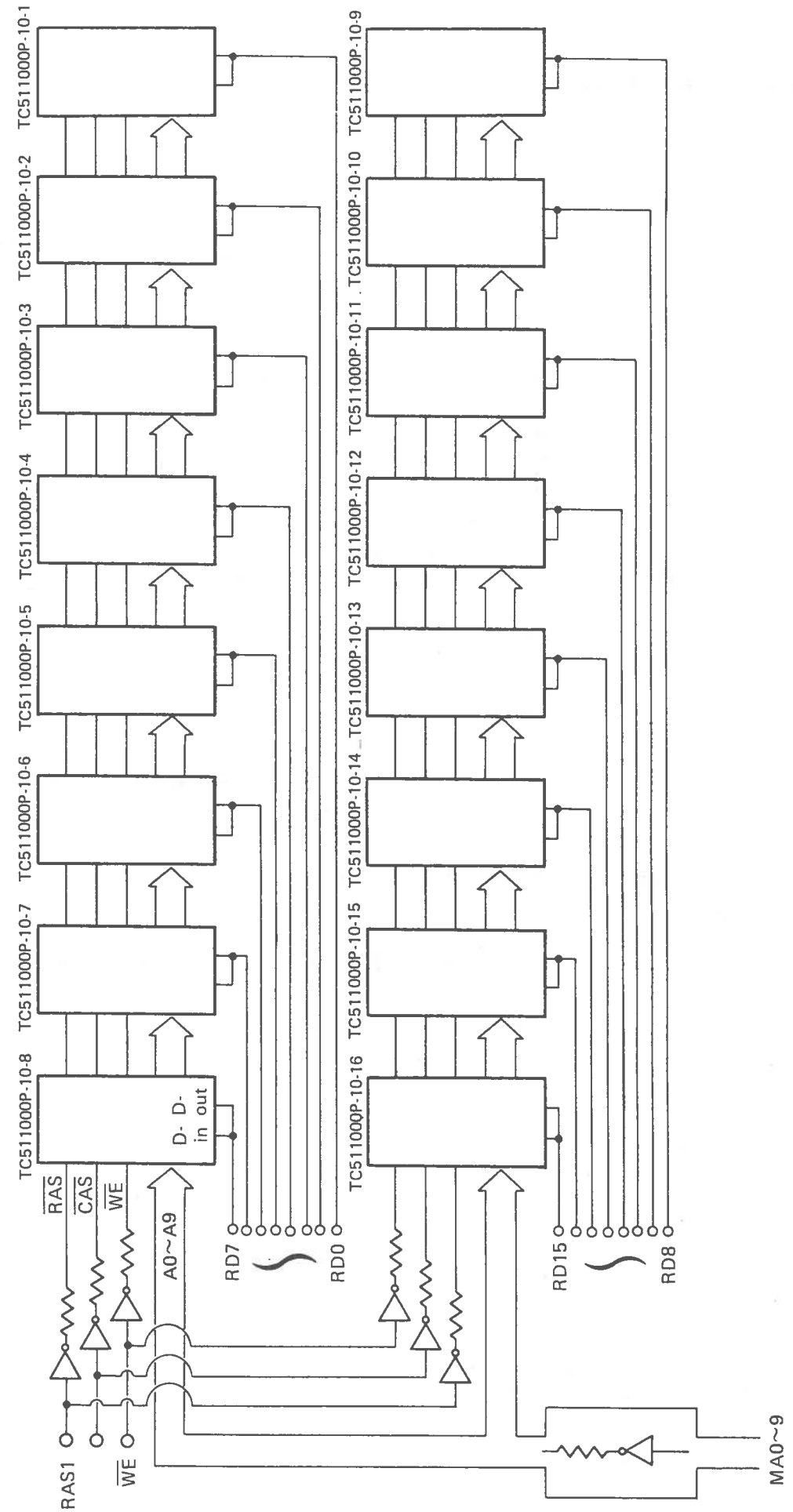
The followings are logic diagram and truth table of bidirectional buffer LS245.



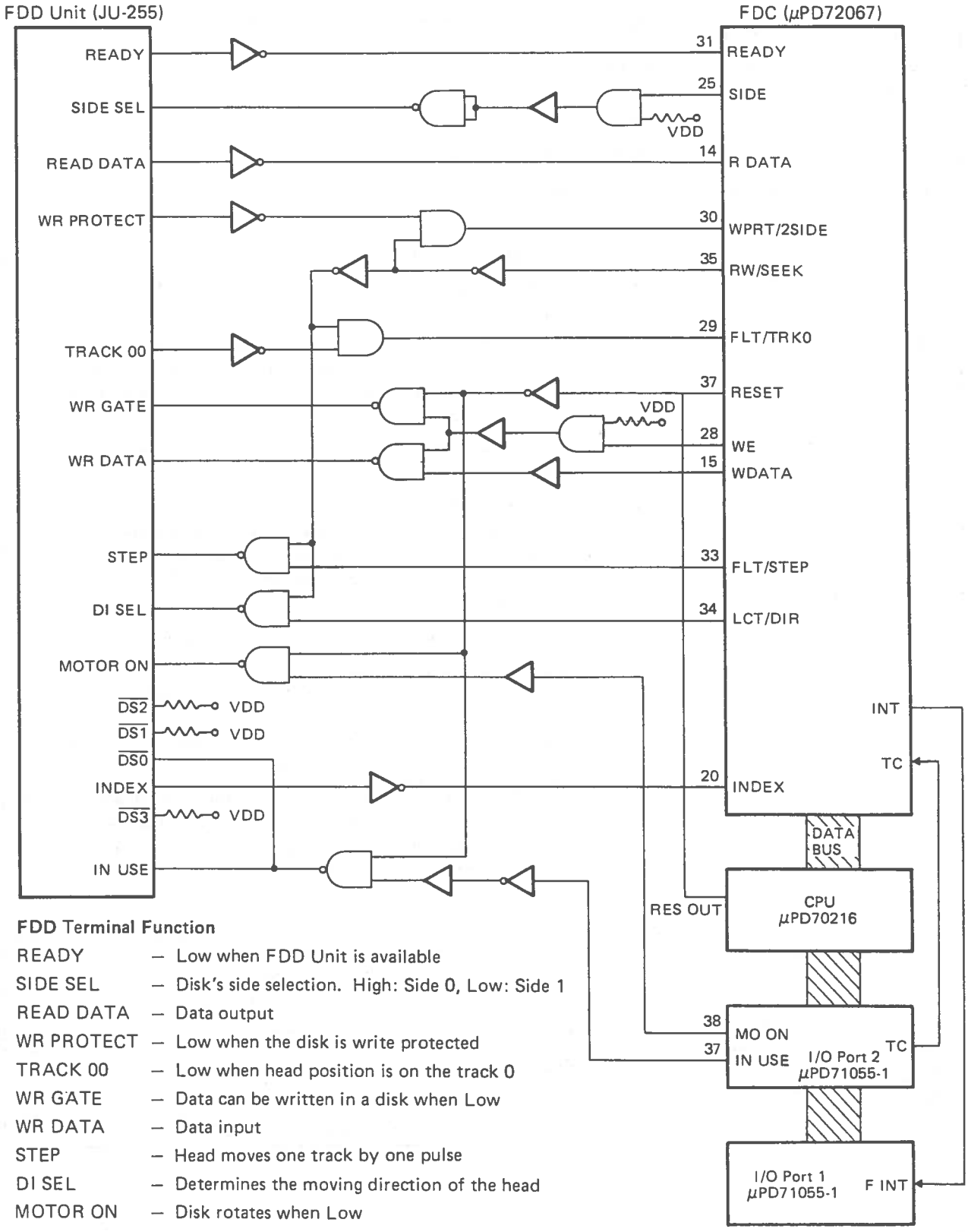
FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H= high level, L= Low level, X= irrelevant


TC511000P-10-1
TC511000P-10-2
TC511000P-10-3
TC511000P-10-4
TC511000P-10-5
TC511000P-10-6
TC511000P-10-7
TC511000P-10-8
TC511000P-10-9
TC511000P-10-10
TC511000P-10-11
TC511000P-10-12
TC511000P-10-13
TC511000P-10-14
TC511000P-10-15
TC511000P-10-16
D- D-
in out
RAS
CAS
WE
A0~A9
RD7
RD0
RD15
RD8
RAS1
WE
MA0~9

FDD (Floppy Disk Drive) INTERFACE



FDD Terminal Function

READY	–	Low when FDD Unit is available
SIDE SEL	–	Disk's side selection. High: Side 0, Low: Side 1
READ DATA	–	Data output
WR PROTECT	–	Low when the disk is write protected
TRACK 00	–	Low when head position is on the track 0
WR GATE	–	Data can be written in a disk when Low
WR DATA	–	Data input
STEP	–	Head moves one track by one pulse
DI SEL	–	Determines the moving direction of the head
MOTOR ON	–	Disk rotates when Low
DS1 ~ DS3	–	Not used
DS0	–	FDD Unit can be operated when Low
INDEX	–	Outputs one pulse per one rotation of disk
IN USE	–	BUSY lamp lights when Low

FDC (Floppy Disk Controller) μPD72067C

Pin No.	Terminal	In/Out	Function
1, 2 48~43	DB7, DB6 DB5 ~ DB0	In/Out	Data bus
5	TC	In	Data transfer complete signal from I/O Port 2
6	INT	Out	Interrupt signal to CPU
10, 11	XA1, XA2	In/Out	32MHz clock pulse
14	R DATA	In	Data input from disk
15	W DATA	Out	Data output to FDD Unit
20	INDEX	In	Receives a signal from FDD Unit when read/write head is at the starting position
25	SIDE	In	As FDD Unit has two driving heads (Head 0 for the top side of disk and Head 1 for the bottom side), this terminal selects either head. When Low, Head 0 is selected whereas Head 1 is assigned when this terminal is High.
28	WE	Out	Write enable. When this terminal is High, data can be written in a disk.
30	WPRT/2 SIDE	In	Write protected or 2-sided disk discrimination terminal. If this terminal receives a signal from FDD Unit while terminal RW/SEEK is Low, FDC discriminates that the disk is write protected. If there is an input at this terminal while RW/SEEK is High, FDC acknowledges that the disk is double sided.
31	READY	In	FDC acknowledges that FDD Unit is available when the terminal receives a signal.
33	FLTR/STEP	Out	FDC outputs FDD error release signal when RW/SEEK terminal is Low. The output from this terminal becomes seek pulse (a signal which moves the driving head) while RW/SEEK is High.
34	LCT/DIR	Out	While RW/SEEK is Low, the output from this terminal acknowledges FDD Unit that the driving head is designated over track 43. When RW/SEEK is high, the voltage level of this terminal determines the moving direction of the head. High . . . . . To outward Low . . . . . To inward
35	RW/SEEK	Out	Discrimination terminal of read/write or seek. High . . . . . Read or write Low . . . . . Seek (moving the head)
37	RESET	In	Power ON reset signal input (Low active)
38	$\overline{RD}$	In	Receives Low level signal when CPU reads data from FDC
39	$\overline{WR}$	In	Receives Low level signal when CPU writes data in FDC
40	$\overline{CS}$	In	While Low, data transfer between FDC and CPU is possible

FDD (Floppy Disc Drive) UNIT JU-255

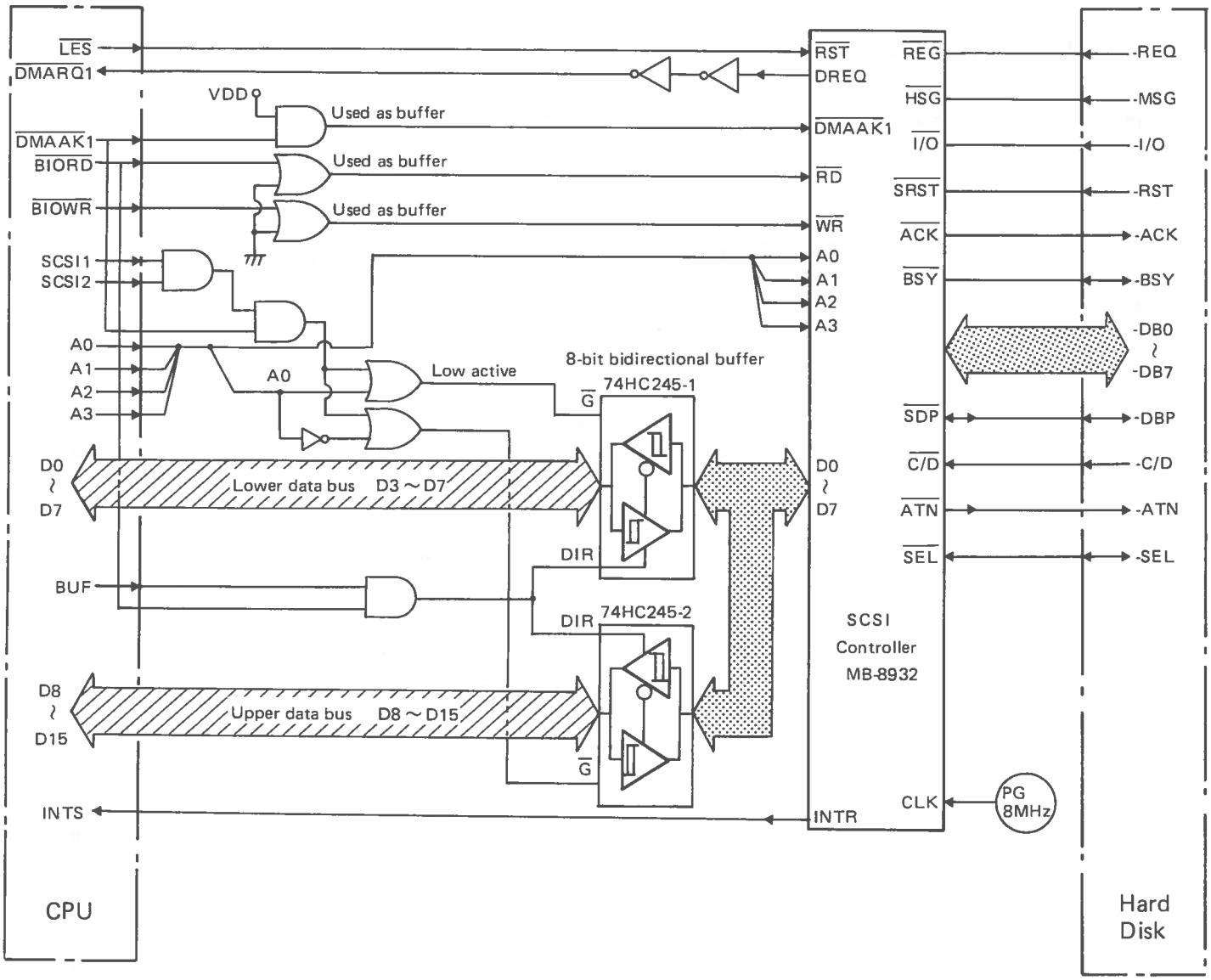
JU-255 is a 3.5 inch double density micro floppy disc drive unit featuring 1.6 Megabyte maximum capacity.

Signal functions of FDD Unit's connector

Terminal Pin No.	Signal	In/Out	Function
4	$\overline{\text{IN USE}}$	In	Low level of this terminal lights the "BUSY" lamp of the FDD Unit
6	$\overline{\text{DB3}}$	In	Not used
8	$\overline{\text{INDEX}}$	Out	Outputs a Low level signal per one rotation of a floppy disc
10	$\overline{\text{DS0}}$	In	Drive 0 selection signal. Connected to $\overline{\text{IN USE}}$ terminal.
12, 14	$\overline{\text{DS1}}$, $\overline{\text{DS2}}$	In	Drive 1 and 2 selection terminals. As JU-386 drives only one disc, these terminals are not used.
16	$\overline{\text{MOTOR ON}}$	In	Motor rotates if this terminal becomes Low while a floppy disc is loaded
18	$\overline{\text{DI SEL}}$	In	Driving head's moving direction select signal input. High ——— To outward Low ——— To inward
20	$\overline{\text{STEP}}$	In	Driving head seeks one track in the direction selected by $\overline{\text{DI SEL}}$ terminal. Head moves at the rising edge of this signal.
22	$\overline{\text{WR DATA}}$	In	Write data timing signal input. Writes data at the falling edge of this terminal.
24	$\overline{\text{WR GATE}}$	In	Data can be written in a floppy disc while this terminal is Low.
26	$\overline{\text{TRACK 00}}$	In	Falls to Low when track 00 is detected
28	$\overline{\text{WR PROTECT}}$	Out	Falls to Low when the loaded disc is write protected or double density sheet
30	$\overline{\text{READ DATA}}$	Out	Outputs data written on the floppy disc
32	$\overline{\text{SIDE SEL}}$	In	Driving head's side selection terminal. High ——— Side 0 (Top) Low ——— Side 1 (Bottom)
34	$\overline{\text{READY}}$	Out	Falls to Low if the following conditions are satisfied. (1) All the voltages are supplied (2) Floppy disc's rotation is over 84 percent of the normal rotation speed (3) A floppy disc is loaded (4) $\overline{\text{DI SEL}}$ terminal is Low (5) Driving head is on track 00 at Power ON

SCASI INTERFACE CIRCUIT

The circuit converts CPU data into SCSI (Small Computer System Interface) data or vice versa.



Since data bus of hard disk is 8-bit, CPU data bus D0 ~ D15 is separated in half by signal A0. While signal A0 is Low, lower data bus D0 ~ D7 become effective whereas upper data is sent (or received) to (from) the hard disk if A0 is high.

Direction of data flow is determined by the voltage level of terminal DIR of 74HC245.

DIR = High ..... CPU ⇨ Hard disk
DIR = Low ..... CPU ⇦ Hard disk

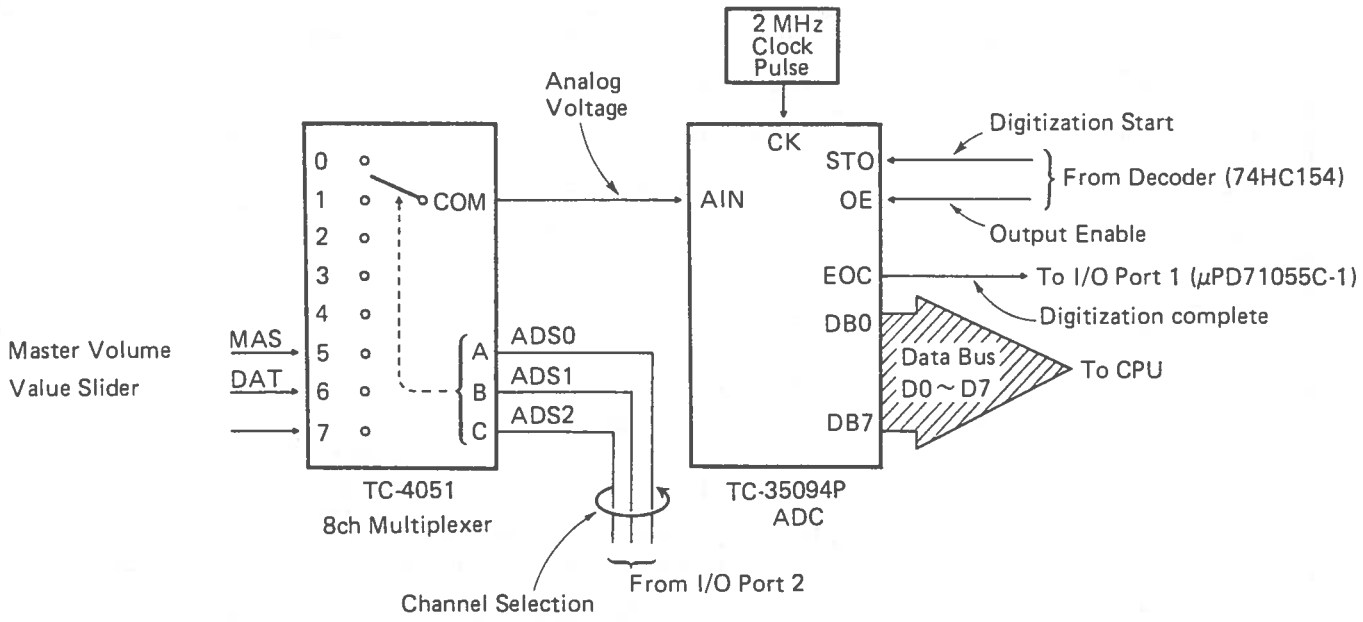
Signals SCSI1 and SCSI2 are used to enable bidirectional buffer 74HC245.

PIN FUNCTIONS OF SCSI CONTROLLER (MB8932)

Pin No.	Terminal	Signal	In/Out	Function
1	$\overline{RST}$	$\overline{RES}$	In	Reset signal. Low active.
2	$\overline{CS}$	SCSI	In	Chip select signal. Low active.
3 ~ 6	A0 ~ A3	A0 ~ A3	In	Selection signals for internal registers.
7 ~ 17	$\overline{SD7}$ ~ $\overline{SD0}$	$\overline{DB7}$ ~ $\overline{DB0}$	In/Out	Hard disk data bus.
18	$\overline{SDP}$	$\overline{DBP}$	In/Out	Parity bit for hard disk data bus. (Odd number parity).
21 ~ 29	D0 ~ D7	DS0 ~ DS7	In/Out	CPU data bus.
30	INTR	INTS	Out	Interrupt to CPU.
31	$\overline{SRST}$	$\overline{RST}$	Out	Reset signal for hard disk.
32	$\overline{BSY}$	$\overline{BSY}$	In/Out	Busy signal between SCSI Controller and hard disk.
34	$\overline{SEL}$	$\overline{SEL}$	In/Out	Drops to Low level when FZ-20M designates a hard disk.
35	$\overline{I/O}$	$\overline{I/O}$	In/Out	Data flow direction select signal. Low . . . . . hard disk ⇨ FZ-20M High . . . . . FZ-20M ⇨ Hard disk
36	$\overline{CD}$	$\overline{CD}$	In/Out	Command/data selection terminal. When Low, the content in data bus is recognized as a command.
38	$\overline{MSG}$	$\overline{MSG}$	In/Out	Drops to Low level when the content in data bus is a "MESSAGE" such as "COMMAND COMPLETE" or "INITIATOR (FZ-20M) DETECTED ERROR"
39	$\overline{REQ}$	$\overline{REQ}$	In/Out	Drops to Low level when hard disk requests data.
41	$\overline{ACK}$	$\overline{ACK}$	In/Out	Acknowledge signal for responding to data request from hard disk.
42	$\overline{ATN}$	$\overline{ATN}$	In/Out	FZ-20M informs hard disk through this terminal that it is going to send messages.
43	$\overline{RD}$	$\overline{BIORD}$	In	Drops to Low when FZ-20M CPU reads data from hard disk.
44	$\overline{WR}$	$\overline{BIOWR}$	In	Drops to Low when FZ-20M CPU writes data in hard disk.
45	DREQ	$\overline{DMARQ1}$	Out	High level when SCSI Controller requests data to CPU.
46	$\overline{DACK}$	$\overline{DMAAK1}$	In	Receives Low level signal when CPU accepts data request.
47	$\overline{CLK}$		In	8 MHz clock pulse input.

8-BIT ADC (TC-35094)

The ADC (Analog to Digital Converter) varies the voltage levels from Master volume control and VALUE pots into digital values.



As one ADC receives inputs from different pots, an 8-channel multiplexer selects one input. Input channel is assigned by voltage combinations of terminals A, B, and C and outputs from terminal COM.

A	B	C	ON Channel	Input Signal
Low	Low	Low	0	Not used
High	Low	Low	1	Not used
Low	High	Low	2	Not used
High	High	Low	3	Not used
Low	Low	High	4	Not used
High	Low	High	5	From Master Volume Control
Low	High	High	6	From VALUE Slider
High	High	High	7	Not used

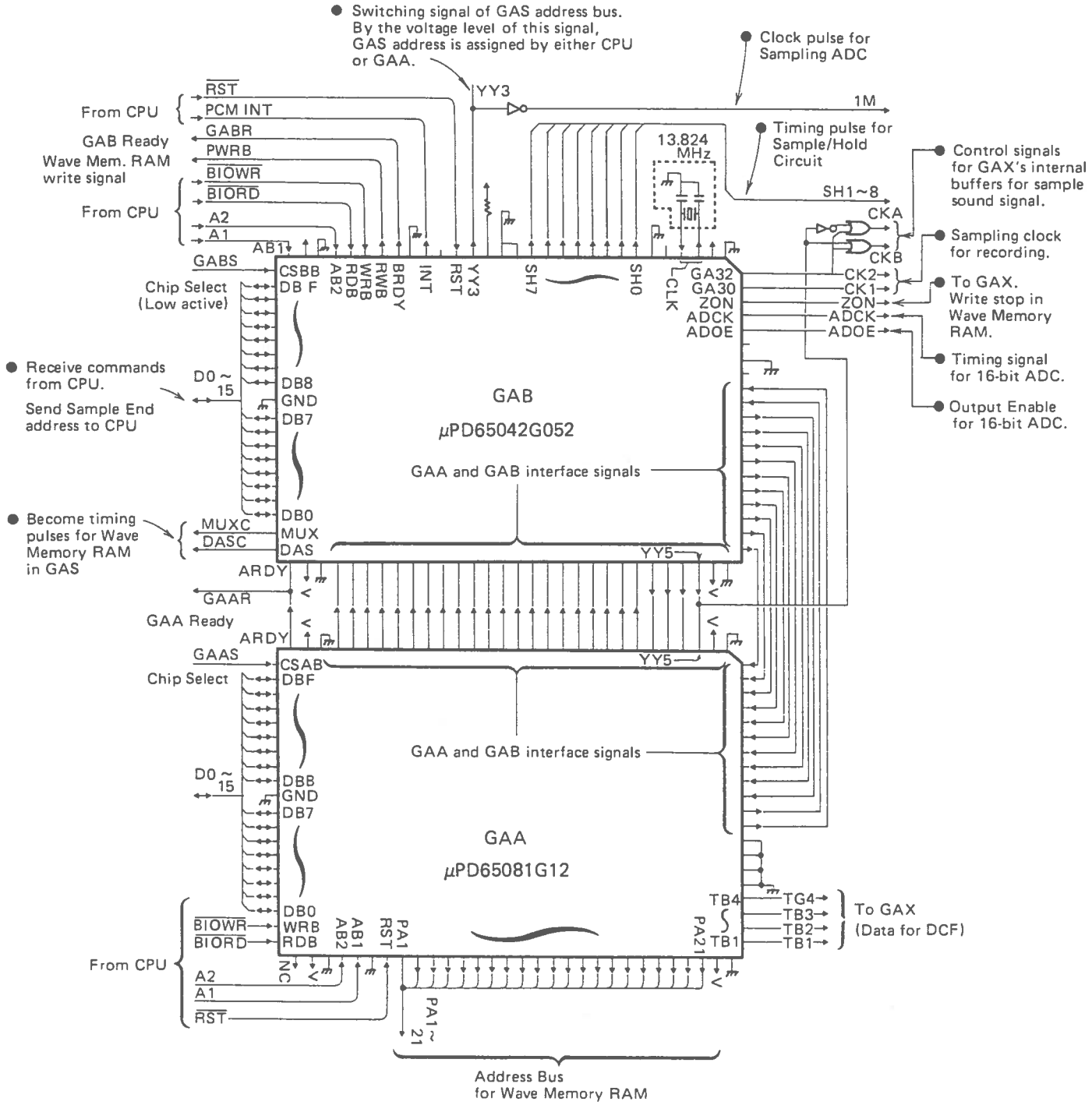
When terminal STO rises to High level, the ADC digitizes the input voltage from terminal A IN and if the digitization is completed, it provides High level signal to I/O Port 1 from terminal EOC. The digitized data are output to CPU via data bus DB0 ~ DB7 when terminal OE is High.

GAA (μPD65081G12) & GAB (μPD65042G052)

Receiving commands from CPU data bus, gate arrays GAA and GAB access the address (start address, end address, loop start address, loop end address etc. . . .) of the Memory RAM via gate array GAS for recording and playbacking of sample sounds.

By means of varing the reading speed of Memory RAM data, those gate arrays vary the pitch of the sounds.

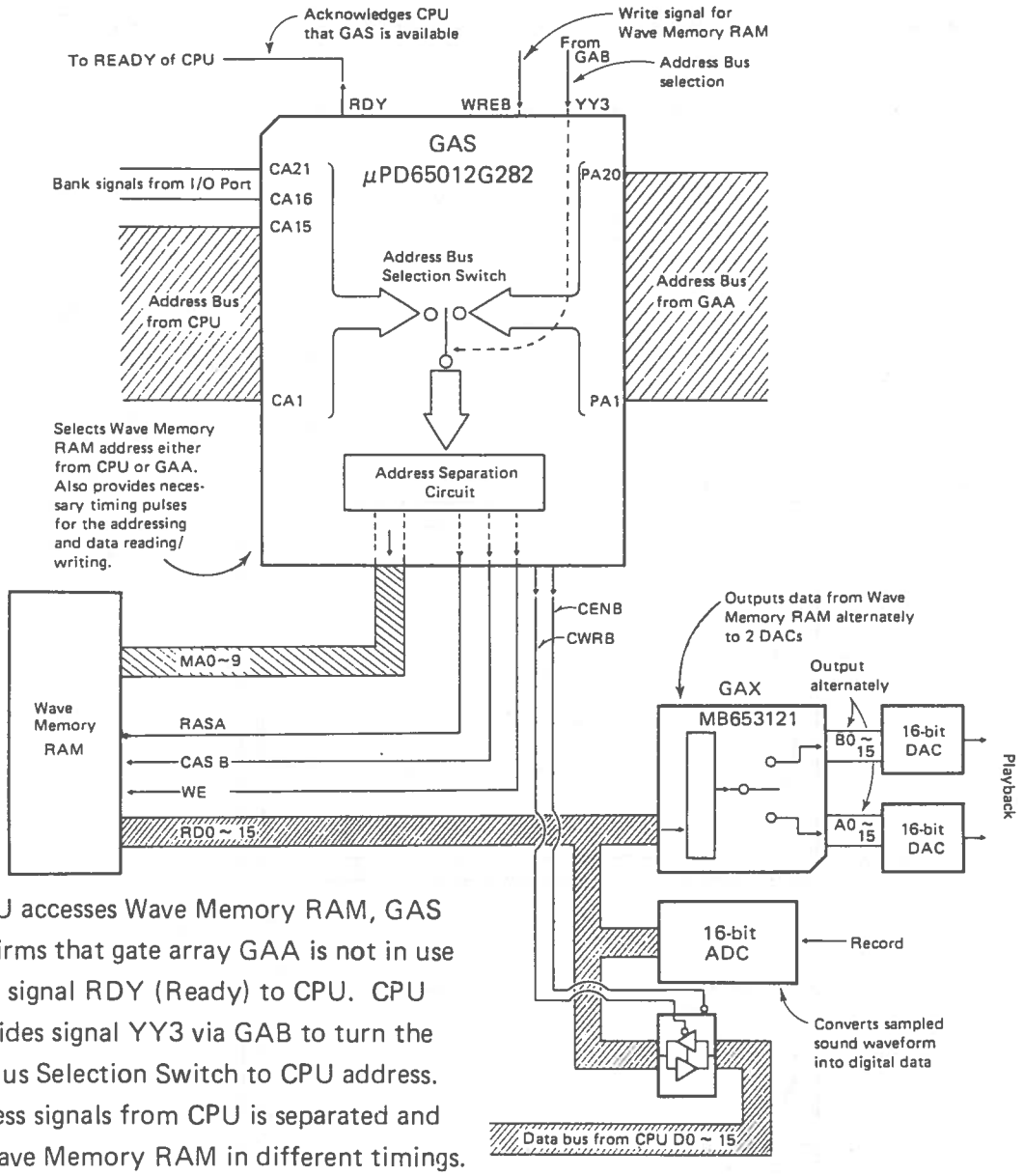
GAA and GAB also provide timing pulses for Sample/Hold Circuit.



GATE ARRAYS GAS (μPD65012G282) & GAX (MB653121)

GAS selects Wave Memory RAM address either from CPU or GAA by turning Address Bus Selection Switch.

Also GAS provides necessary timing signals for the addressing.



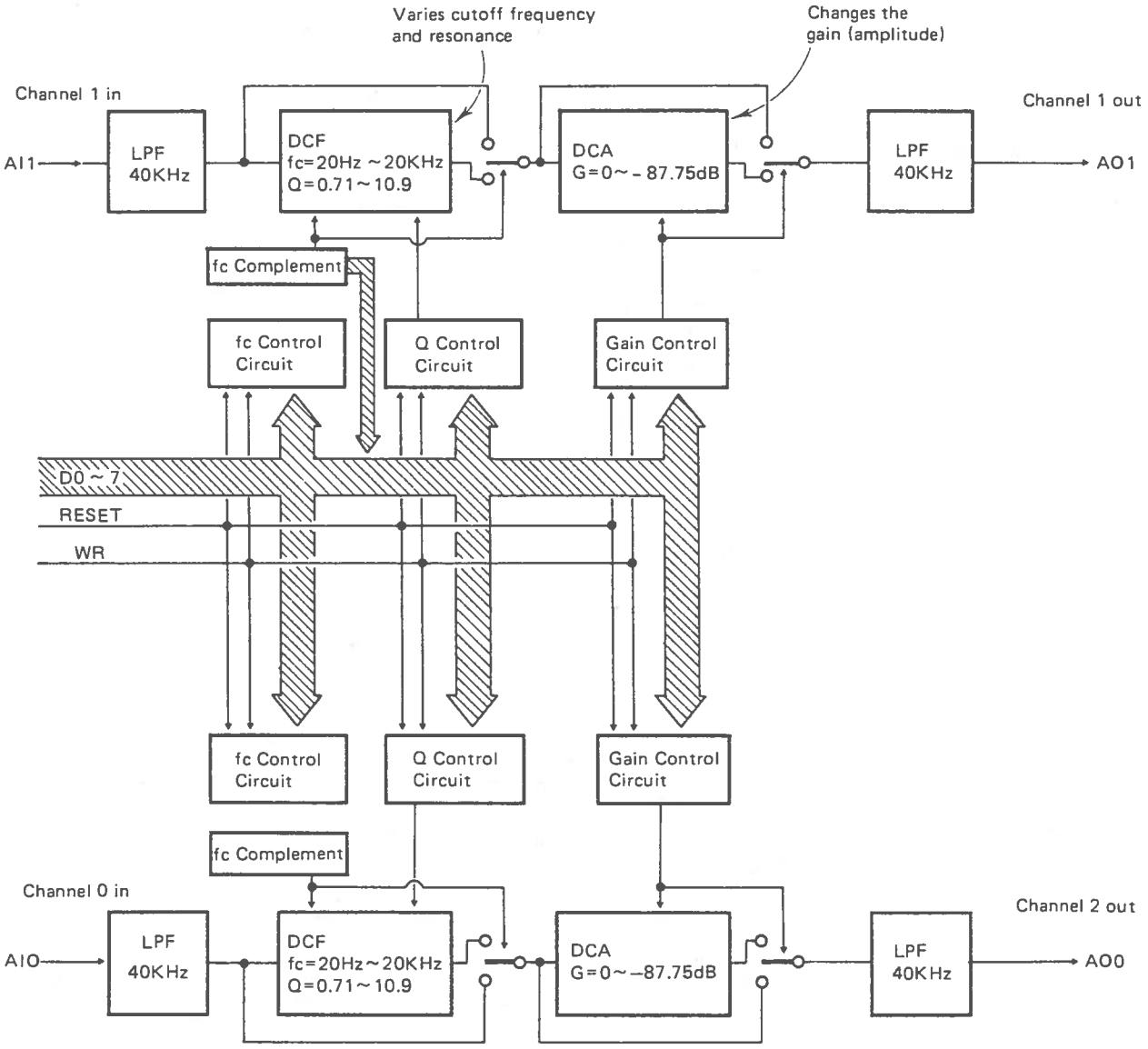
When CPU accesses Wave Memory RAM, GAS first confirms that gate array GAA is not in use then send signal RDY (Ready) to CPU. CPU then provides signal YY3 via GAB to turn the Address Bus Selection Switch to CPU address. The address signals from CPU is separated and sent to Wave Memory RAM in different timings. Providing signals CENB and CWRW to the bidirectional buffer, GAS controls the direction of data flow.

When sampling a sound, gate array GAA assigns Wave Memory RAM address. Sampled sound is digitized in the 16-bit ADC (Analog to Digital Converter) and stored in the assigned address in Wave Memory RAM.

For playbacking the stored sound, GAA assigns Wave Memory RAM address and sends data from the Wave Memory RAM into gate array GAX.

GAX eliminates a harmonic noise contained in data signals and sends the noise free data to two 16-bit DACs (Digital to Analog Converters) alternately.

DCF (MB87186)

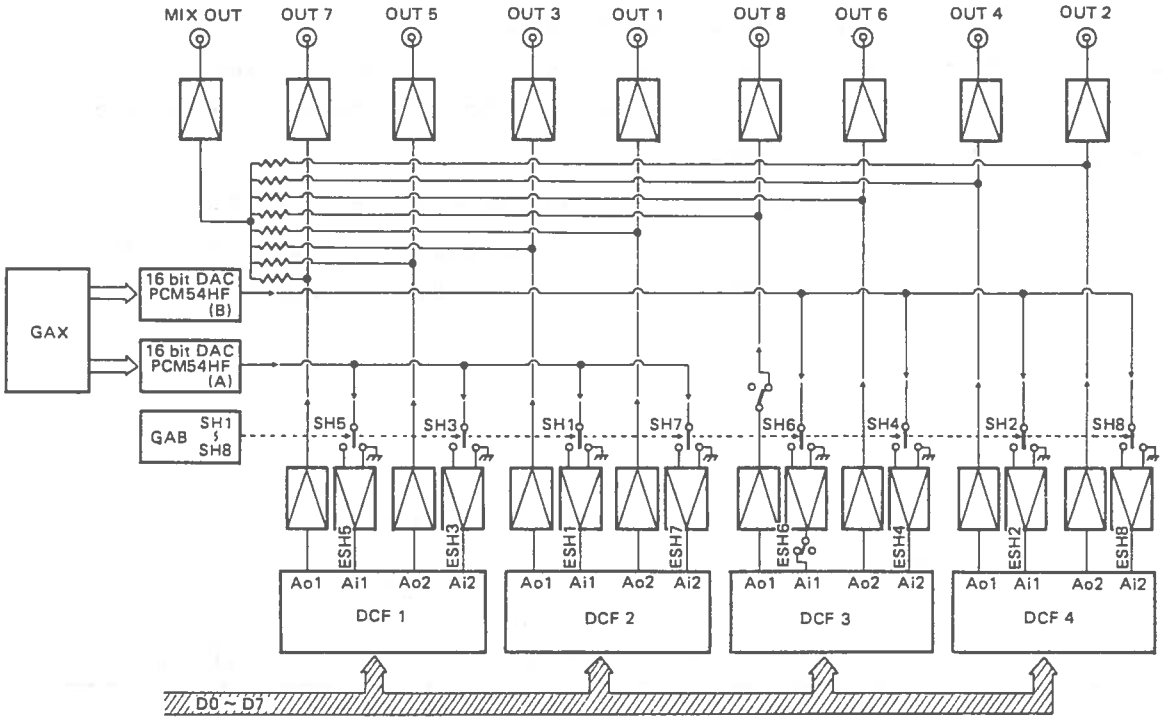


Block Diagram of MB87186

MB87186 contains two each of DCF (Digital Controlled Filter) and DCA (Digital Controlled Amplifier) which vary cutoff frequency, resonance, and amplitude of sound signals.

Pin No.	Terminal	In/Out	Function
1 ~ 8	D0 ~ D7	In	Digital data for cutoff frequency, resonance, and amplitude values
9	$\overline{WR}$	In	Data write signal (Low active)
10	$\overline{CE}$	In	Chip enable signal (Low active). Connected to the ground.
11	CHS	In	Channel selection signal. High level designates channel 1 while channel 2 is selected by being Low of this terminal.
12	F/A	In	Filter/Amp switching signal. When this terminal is High, signals of data bus become DCF control data and being Low makes them amplitude control data.
13	FC/Q	In	Cutoff frequency/Resonance selection signal. When terminal F/A (pin 12) and this terminal are High level, input data determines cutoff frequency in DCF. If this terminal is High while F/A is Low, upper 2 bits of the data bus become gain control data in DCA. While both F/A and FC/Q are Low, all the 8 bits of the data bus determines the amplitude value in DCA.
14	DG	—	Digital ground
15~7	—	—	Not used
18	OSC I	In	3.58MHz clock pulse. Data are written in at the rising edge (_┐‾) of this clock pulse.
19	$\overline{RESET}$	In	Being Low of this terminal sets values of VCF and VCA as follows. Cutoff Frequency : 20 Hz Resonance : 0.71 Gain : — ∞dB
20	VSS	—	-5V source
21	AI2	In	Source sound signal input for channel 2
22	$\overline{PD}$	In	Power down control terminal (not used)
23	AO2	Out	Filtered and amplified sound output of channel 2
24	AG	—	Ground source for the internal linear circuit
25	AO1	Out	Filtered and amplified sound output of channel 1
26	$\overline{TC}$	In	Not used (Connected to +5V)
27	AI1	In	Source sound signal input for channel 1
28	VDD	—	+5V source

PLAYBACK CIRCUIT



Receiving data from CPU, DCFs set cutoff frequency, resonance, and amplitude values. Sampled sound data stored in Wave Memory RAM enter 16-bit DACs PCM54HF (A) and (B) alternately via gate array GAX.

Since single output of a 16-bit DAC is 4-channel multiplex signal (four kinds of sounds are combined by time sharing), signals SH1 ~ SH8 from gate array GAB separate the multichannel signal into single sound signals.

Each sound is filtered and gain-controlled in a DCF and output to a parallel line out terminal via two op amps.

MIX OUT terminal outputs all the sound signals from OUT 1 to OUT 8 terminals.

SAMPLING

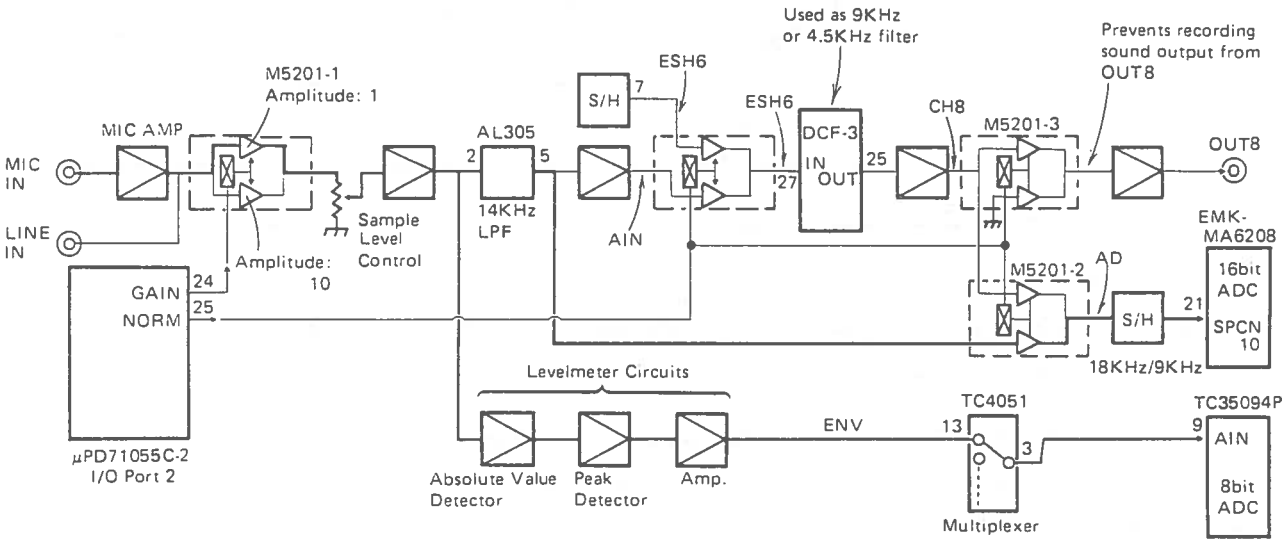
The FZ-20M is able to select three sampling frequencies 36KHz, 18KHz, and 9KHz and also be able to choose the recording gain of HIGH or LOW.

To sample a sound, double higher frequency of the maximum frequency of recording sound is necessary. Namely, if the maximum frequency of a recording sound is 5KHz, it is necessary to sample the sound with at least 10KHz sampling frequency.
Because a noise may be generated when the recording sound's frequency exceeds a half of the sampling frequency, FZ-20M passes the recording sound through a low-pass filter whose cutoff frequency is a half of the sampling frequency.

Sampling frequency : 36KHz —— Cutoff frequency of low-pass filter: 18 KHz
Sampling frequency : 18KHz —— Cutoff frequency of low-pass filter: 9 KHz
Sampling frequency : 9KHz —— Cutoff frequency of low-pass filter: 4.5 KHz

(1) Signal flow of 36 KHz sampling

Gain: LOW

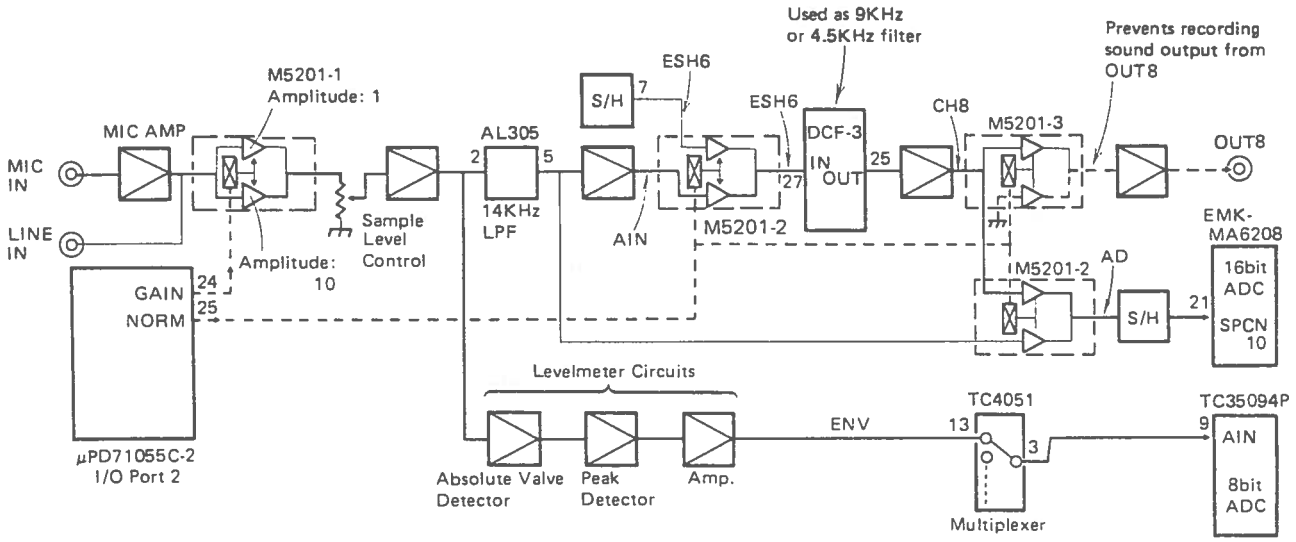


When recording a sound from MIC input, the input signal is amplified by the MIC Amp and if the input is from LINE IN, it directly enters a switching op amp M5201. M5201 contains two op amps whose amplitudes are 1 and 10.
Depends on the Sampling Level setting, the recording sound passes either one of the op amps. This switching of the op amps is made by the signal GAIN from I/O Port 2's pin 24.

After passing Sample Level Control VR and one op amp, the signal enters 14KHz low-pass filter. Although the cutoff frequency of the filter is 14KHz, it shuts the signal over 18KHz since the slope of the cutoff frequency response is gentle.

For displaying the sampling level on the LCD, the unfiltered sound signal passes Absolute Volume Detector which detects the mean value of the sound volume, Peak Detector that extracts the maximum sound level, and an amplifier. After then, the sound level signal passes Multiplexer TC4051, digitized in 8-bit ADC, and sent to the CPU as sound level data.

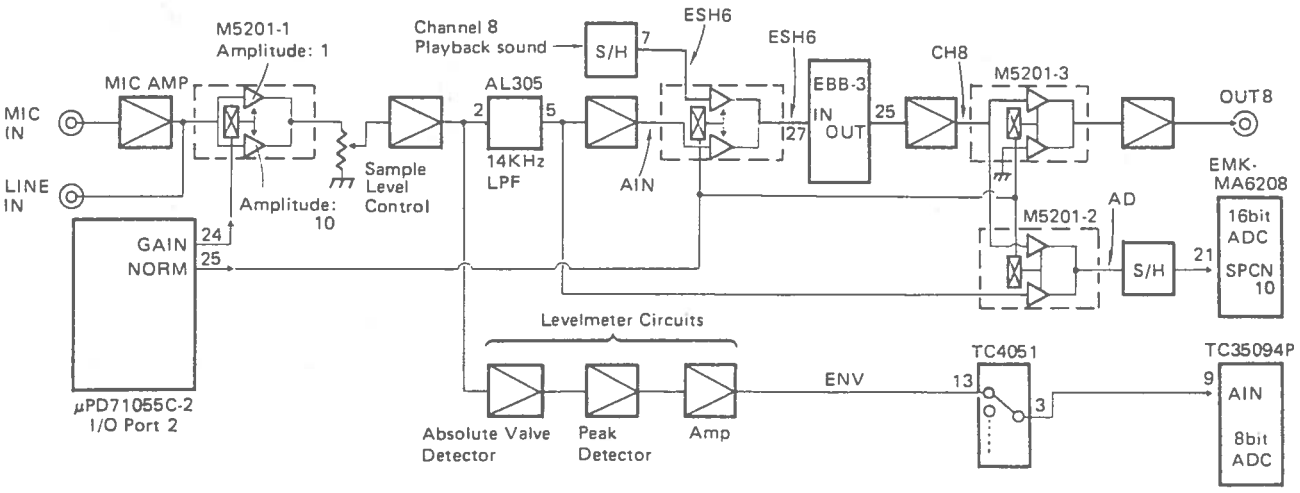
(2) Signal flow of 18KHz or 9KHz sampling (Sampling Gain: HIGH)



After passing 14KHz LPF and an amplifier, the recording sound signal enters a switching op amp M5201-2 in MA1M PC Board.
By signal NORM, the switching op amp sends the sound signal to DCF 3.
Although DCFs are normally used for filtering playback sounds, channel 1 of DCF 3 is also utilized to filter recording sounds.
Depends on the sampling frequency setting, CPU sends 9KHz or 4.5KHz cutoff data to DCF3. 9KHz or 4.5KHz filtered sound is provided to 16-bit ADC via an amplifier, M5201-2 in MA2M PCB, and S/H circuit.

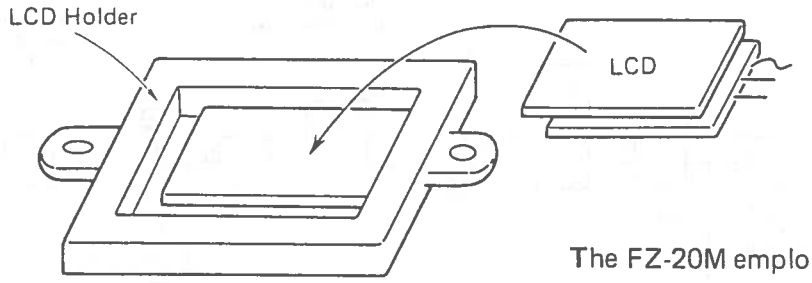
Since channel 1 output of DCF 3 is connected to OUT 8 output jack, signal NORM also cuts the sound signal off in M5201-3 to prevent outputting the recording sound from OUT 8.

(3) Playback from OUT 8



After recording of a sample sound, signal NORM turns switching op amp M5201-3 on so that OUT 8 is able to output playback sounds.

LCD UNIT

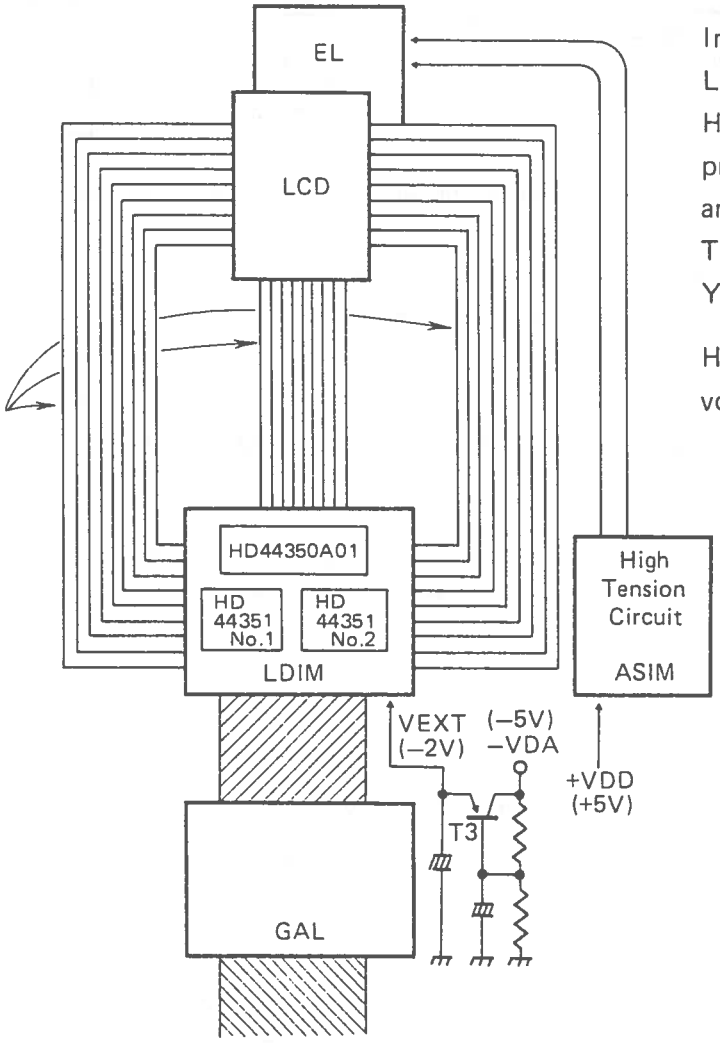


The FZ-20M employes 64x96 dots graphic LCD.

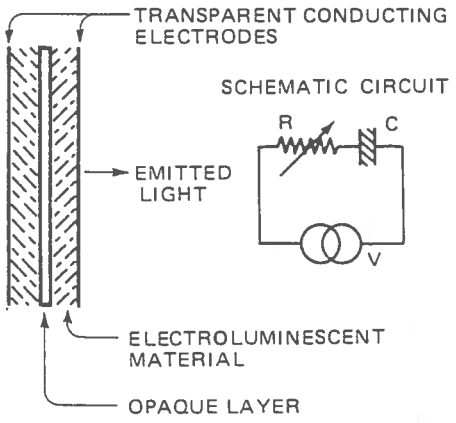
Gate array GAL converts the CPU data language into LCD Drivers' data word.

In the LCD Drive PCB, there are three control LSIs HD44350A01 and two HD44351s. HD44350A01 contains character generator and provides common signals X1 ~ X32, Z1 ~ Z16, and W1 ~ W16 for the LCD.
The two HD44351s generate LCD dot signals Y1 ~ Y80.

High Tension Circuit generates +90 to +100V voltage which is necessary for lighting EL.



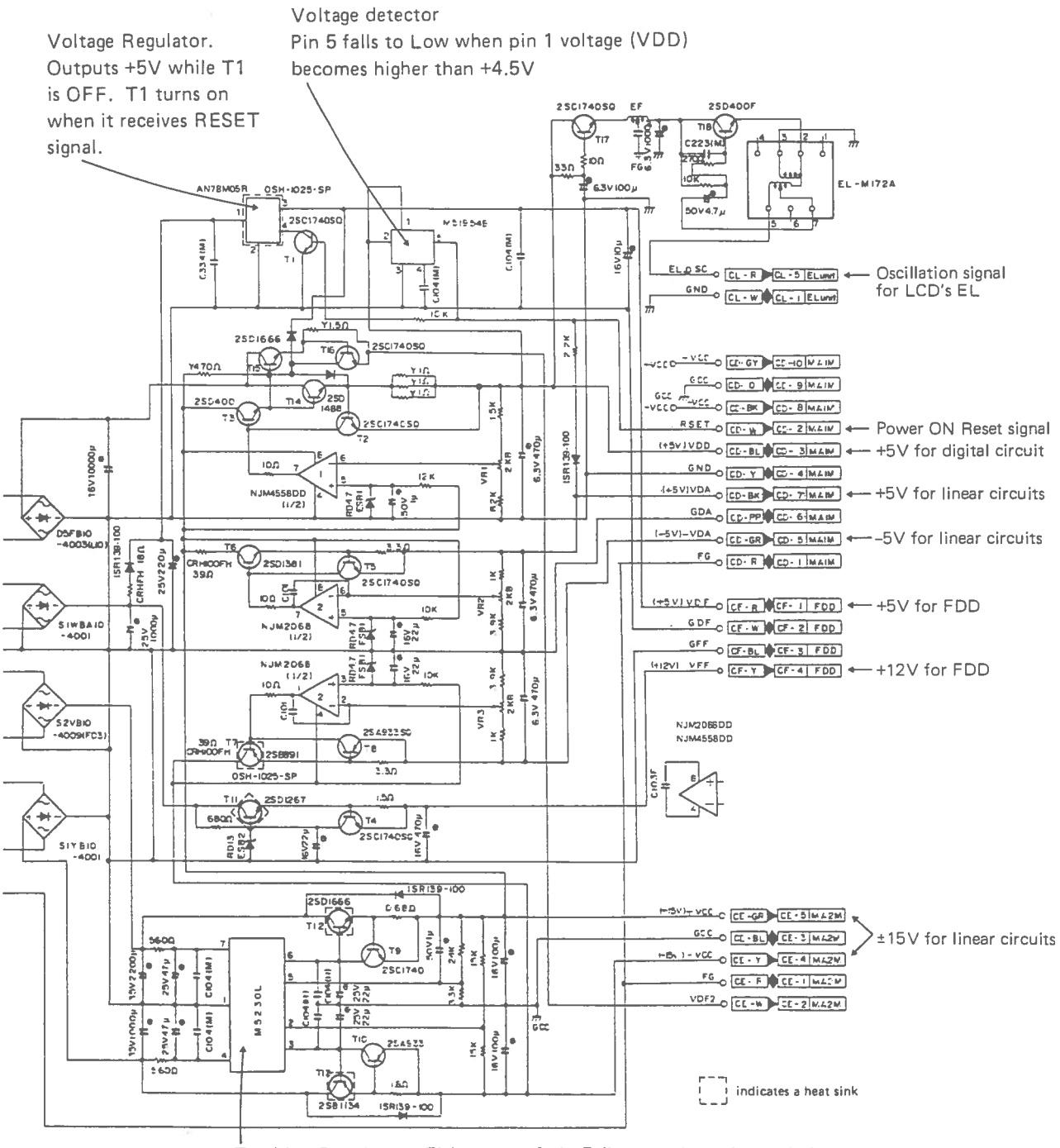
EL (Electroluminescent panel)



Electroluminescence principle. Incident radiation arriving from left passes through transparent electrodes to act on photoconductor (shaded area).

POWER SUPPLY CIRCUIT

This block generates voltages VDD (+5V for digital circuits), -VDD (-5V for digital circuits), VDA (+5V for linear circuits), -VDA (-5V for linear circuits), +VCC (+15V for linear circuits), -VCC (-15V for linear circuits), VDF (+5V for FDD Unit), VFF (+12V for FDD Unit), and Power ON RESET signal.



PARTS LIST

FZ-20M

Notes:

1. Prices and specifications are subject to change without prior notice.
2. As for spare parts order and supply, refer to the "GUIDEBOOK for Spare Parts Supply", published separately.
3. The numbers in item column correspond to the same numbers in drawing.

Item	Code No.	Parts Name	Spec. No.	Q	*	FOB Japan N. R. Yen Unit Price	R N K	
	1) M5307-MAIN PCB ASS'Y							
	2002 1322	LSI	UPD71055C	2			A	G
	2010 1946	LSI	UPD43256C-12L	2			A	O
	2010 2016	LSI	EHK-MA6208	1			A	O
	2010 2023	LSI	MB653121	1			A	K
	2010 2037	LSI	PCM54HP	2			A	E
	2010 2044	LSI	UPD65012C-046	1			A	C
	2010 2058	LSI	UPD65042G-052	1			A	M
	2010 2072	LSI	UPD70216G	1			A	R
	2010 2352	LSI	FM-1	4			A	Q
	2010 3507	LSI	UPD65081GF-012	1			A	W
	2010 5054	LSI	UPD65012G-282-12	1			A	E
	2010 5061	LSI	UPD72067C	1			A	N
O*	2010 6153	LSI	TC511000AP-10	16			A	U
O*	2010 7091	LSI	UPD27C256AD-12MZ3B	1			A	L
O*	2010 7098	LSI	UPD27C256AD-12MZ4B	1			A	L
	2100 3786	C MOS IC	TC40H004P	2			A	B
	2100 4029	C MOS IC	TC4051BP	1			A	C
	2105 0511	C MOS IC	TC35094P	1			A	C
	2105 0595	C MOS IC	UPD4053BC	3			A	B
	2105 1008	C MOS IC	TC74HC00AP	2			A	A
	2105 1085	C MOS IC	TC74HC02AP	1			A	B
	2105 1092	C MOS IC	TC74HC04AP	3			A	B
	2105 1099	C MOS IC	TC74HC32AP	2			A	B
	2105 1162	MOS IC	TC74HC154AP	1			A	B
O*	2105 1169	C MOS IC	TC74HC373AP	3			A	B
O*	2105 1218	C MOS IC	TC74HC08AP	2			A	A
O*	2105 1225	C MOS IC	TC74HC27AP	1			A	A
O*	2105 1232	C MOS IC	TC74HC74AP	1			A	B
O*	2105 1239	C MOS IC	TC74HC164AP	2			A	B
O*	2105 1246	C MOS IC	TC74HCT244AP	2			A	B
O*	2105 1253	C MOS IC	TC74HC368AP	1			A	B
	2110 3756	Bipolar IC	SN74LS04N	2			A	B
	2111 2143	Bipolar IC	SN74LS14N	1			A	D
	2111 2283	Bipolar IC	SN74LS08N	1			A	B
	2111 2496	Bipolar IC	SN74LS174N	1			A	B
	2111 2640	Bipolar IC	SN74LS38N	2			A	B
	2111 2879	Bipolar IC	SN74LS245N	4			A	E
	2111 5215	Bipolar IC	SN74LS367AN	3			A	C
	2111 5291	Bipolar IC	SN74LS139N	1			A	C
	2111 5789	Bipolar IC	SN74LS368AN	1			A	B
	2113 0091	Bipolar IC	MC74F04N	2			A	B
	2114 0021	Monolithic IC	LA6462D	4			A	B
	2114 0224	Monolithic IC	M5201P	1			A	B
	2114 1421	Photo coupler	PC900V	1			A	C
	2116 0007	OP amp	NJM082D	5			A	B
O*	2250 0448	Transistor	2SA1630R-T	1	10		A	A
O*	2252 0476	Transistor	2SC4266R-T	1	10		A	A
	2301 0241	Diode	1SS254T-77-T	6	20		C	A
	2520 1337	Ceramic oscillator	CSA3.58MG	1			A	B
	2520 1469	Ceramic oscillator	CSA2.000MK	1			A	B
O*	2590 0182	Crystal oscillator	NR-18-13.824MHZ	1			A	B
	2590 0203	Ceramic oscillator	CSA16.00MX040	1			A	B
	2590 0469	Crystal oscillator	NR-18-32.000MHZ	1			A	B
	2606 0196	Carbon film resistor	R-20-2.4K-J-T24-T	1	20		C	A
	2606 0490	Carbon film resistor	R-20-5.6-J-T24-T	1	20		C	A
	2617 0028	Carbon film resistor	R-20-100-J-T24-T	9	20		C	A

Notes: O* – New parts
Q'ty – Quantity used per unit
* – Minimum order and supply quantity

Rank A: Essential
B: Stock recommended
C: Others
X: No stock recommended

Item	Code No.	Parts Name	Spec. No.	Q	*	FOB Japan N. R. Yen Unit Price	RNK	
	2617 0036	Carbon film resistor	R-20-220-J-T24-T	6	20		C	A
	2617 0052	Carbon film resistor	R-20-1K-J-T24-T	14	20		C	A
	2617 0079	Carbon film resistor	R-20-3.3K-J-T24-T	16	20		C	A
	2617 0095	Carbon film resistor	R-20-10K-J-T24-T	7	20		C	A
	2617 0109	Carbon film resistor	R-20-33K-J-T24-T	8	20		C	A
	2617 0117	Carbon film resistor	R-20-47K-J-T24-T	3	20		C	A
	2617 0133	Carbon film resistor	R-20-82K-J-T24-T	1	20		C	A
	2617 0141	Carbon film resistor	R-20-100K-J-T24-T	1	20		C	A
	2617 0176	Carbon film resistor	R-20-1M-J-T24-T	2	20		C	A
	2617 0231	Carbon film resistor	R-20-270-J-T24-T	1	20		C	A
	2617 0249	Carbon film resistor	R-20-470-J-T24-T	1	20		C	A
	2617 0271	Carbon film resistor	R-20-5.6K-J-T24-T	1	20		C	A
	2617 0273	Carbon film resistor	R-20-22-J-T24-T	29	20		C	A
	2617 0297	Carbon film resistor	R-20-22K-J-T24-T	1	20		C	A
	2617 0408	Carbon film resistor	R-20-6.8K-J-T24-T	1	20		C	A
	2617 0505	Carbon film resistor	R-20-33-J-T24-T	33	20		C	A
	2617 0877	Carbon film resistor	R-20-8.2K-J-T24-T	16	20		C	A
	2720 4074	Module resistor	MS1037F	1	20		B	A
	2725 0077	Module resistor	MS2228-F	2	10		B	A
	2730 0021	Module resistor	MS1038F	6	10		B	A
	2730 0023	Module resistor	MS1036F	1	10		B	A
O*	2801 8722	Electrolytic capacitor	6.3RA2-100-T2-T	2	10		C	A
O*	2801 8736	Electrolytic capacitor	16RA2-10-T2-T	18	10		C	A
O*	2801 8799	Electrolytic capacitor	10RA2-33-T2-T	1	10		C	A
O*	2801 8806	Electrolytic capacitor	6.3RA2-47-T2-T	14	10		C	A
	2807 0276	Electrolytic capacitor	50RNBBP1-T2-T	8	10		C	A
	2813 0637	Semi conductive capacitor	DD308F224Z12-T	16	20		C	A
	2818 0403	Ceramic capacitor	RT-HE60TKYB222K-T	1	10		C	A
	2818 0446	Ceramic capacitor	RT-HE40TKYB101K-T	6	10		C	A
	2818 2082	Ceramic capacitor	RT-HE70TKYF103Z-T	81	10		C	A
	2818 3208	Ceramic capacitor	RT-HE50TKCH330J-T	3	10		C	A
	2818 3224	Ceramic capacitor	RT-HE40TKCH150J-T	2	10		C	A
	2818 3241	Ceramic capacitor	RT-HE80TKCH101J-T	2	10		C	A
	2818 3283	Ceramic capacitor	RT-HE50TKCH300J-T	2	10		C	A
	2818 3313	Ceramic capacitor	RT-HE40TKCH100D-T	1	20		C	A
	2818 3321	Ceramic capacitor	RT-HE60TKCH470J-T	3	20		C	A
O*	2818 3534	Ceramic capacitor	RT-HE12TKSL102K-T	1	10		C	A
	2819 0450	Ceramic capacitor	RT-HE70TKSL221K-T	8	10		C	A
	2819 0531	Ceramic capacitor	RT-HE80TKSL331K-T	8	10		C	A
	2830 6229	Mylar capacitor	AMZV-104K50-T	4	10		C	A
	2830 6296	Mylar capacitor	AMZV-332K50-T	1	10		C	A
	2830 6312	Mylar capacitor	AMZV-471K50-T	1	10		C	A
	2830 6410	Mylar capacitor	AMZV-823K50-T	8	10		C	A
	2830 6550	Mylar capacitor	AMZV-182K50-T	1	10		C	A
	2845 0280	Ferrite beads	EXC-ELDR35C	43	20		C	A
	3013 0175	SB coil	STB-060	6			C	B
	3025 0203	EMI filter	EXC-EMT222DC	19			C	A
	3500 3355	Pin assembly 3P	IL-G-3P-S3T2-E	1	10		X	A
	3500 3401	Connector 4P	IL-G-4P-S3T2-E	2			X	A
	3500 3673	Pin assembly 10P	IL-G-10P-S3T2-E	1			X	A
	3500 7075	PCB connector	5229-19CPB	1			X	B
	3501 1078	D sub connector	DBLC-J25SAF-10L6	1			X	C
	3501 3010	15P connector M306A	IL-15P-19-M306	1			X	C
O*	3501 3661	Header	D3431-6002SCSC	1			X	C
O*	3501 3668	Header	3440-6002SCSC	1			X	C
	3511 1409	PCB connector	5229-11CPB	1			X	A
	3612 0541	DIN jack	TCS4650-01-1211	3			X	B

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O*	3841 0483	Inductor	ELE-Y1ROKA	1			C	A
O*	4317 0350	Blank PCB M5307-MA1M	M10452-1	1			X	Z
O*	4317 0360	Blank PCB M5307-MA3M	M10452-2	1			X	B
O*	4317 0370	Blannk PCB M5307-MA4M	M10452-3	1			X	B
	2) M5306-MA2M PCB ASS'Y							
	2114 0021	Monolithic IC	LA6462D	7			A	B
	2114 0224	Monolithic IC	M5201P	3			A	B
	2114 0343	Monolithic IC	UPC1213C	1			A	B
	2121 0013	OP amp	NJM4558DD	2			A	B
	2220 1387	Transistor	2SC1740SQ-TP-T	3	10		A	A
	2253 0154	Transistor	2SD1381Q,R	2	10		A	A
	2301 0241	Diode	1SS254T-77-T	6	20		C	A
	2360 0007	Zener diode	RD10ESB1-T1-T	1	20		B	A
O*	2606 0077	Carbon film resistor	R-20-620-J-T24-T	2	20		C	A
	2617 0028	Carbon film resistor	R-20-100-J-T24-T	5	20		C	A
	2617 0052	Carbon film resistor	R-20-1K-J-T24-T	27	20		C	A
	2617 0095	Carbon film resistor	R-20-10K-J-T24-T	12	20		C	A
	2617 0109	Carbon film resistor	R-20-33K-J-T24-T	3	20		C	A
	2617 0117	Carbon film resistor	R-20-47K-J-T24-T	8	20		C	A
	2617 0141	Carbon film resistor	R-20-100K-J-T24-T	16	20		C	A
	2617 0168	Carbon film resistor	R-20-220K-J-T24-T	1	20		C	A
	2617 0192	Carbon film resistor	R-20-1.8K-J-T24-T	2	20		C	A
	2617 0203	Carbon film resistor	R-20-470K-J-T24-T	2	20		C	A
	2617 0214	Carbon film resistor	R-20-2.7K-J-T24-T	2	20		C	A
	2617 0220	Carbon film resistor	R-20-150-J-T24-T	1	20		C	A
	2617 0246	Carbon film resistor	R-20-12K-J-T24-T	1	20		C	A
	2617 0265	Carbon film resistor	R-20-10-J-T24-T	1	20		C	A
	2617 0289	Carbon film resistor	R-20-15K-J-T24-T	1	20		C	A
	2617 0297	Carbon film resistor	R-20-22K-J-T24-T	16	20		C	A
	2617 0424	Carbon film resistor	R-20-820K-J-T24-T	1	20		C	A
	2617 0459	Carbon film resistor	R-20-27K-J-T24-T	2	20		C	A
	2617 0475	Carbon film resistor	R-20-50K-J-T24-T	2	20		C	A
	2617 0877	Carbon film resistor	R-20-8.2K-J-T24-T	1	20		C	A
O*	2617 1020	Carbon film resistor	R-20-75K-J-T24-T	3	20		C	A
O*	2801 8680	Electrolytic capacitor	6.3RA2-33-T2-T	2			C	A
O*	2801 8687	Electrolytic capacitor	10RA2-22-T2-T	1			C	A
O*	2801 8694	Electrolytic capacitor	16RA2-100-T2-T	3			C	A
O*	2801 8701	Electrolytic capacitor	10RA2-47-T2-T	1			C	A
O*	2801 8708	Electrolytic capacitor	50RA2-3R3-T2-T	1			C	A
O*	2801 8715	Electrolytic capacitor	10RA2-100-T2-T	3			C	A
O*	2801 8729	Electrolytic capacitor	6.3RA2-220-T2-T	1			C	A
O*	2801 8736	Electrolytic capacitor	16RA2-10-T2-T	1			C	A
	2807 0276	Electrolytic capacitor	50RNBBP1-T2-T	16	10		C	A
	2807 0501	Electrolytic capacitor	16RNBBP10-T2-T	2	10		C	A
	2818 0365	Ceramic capacitor	RT-HE50TKYB102K-T	3	10		C	A
	2818 2082	Ceramic capacitor	RT-HE70TKYF103Z-T	19	10		C	A
	2818 3313	Ceramic capacitor	RT-HE40TKCH100D-T	1	20		C	A
	2819 0425	Ceramic capacitor	RT-HE40TKSL330K-T	2	10		C	A
	2819 0557	Ceramic capacitor	RT-HE50TKSL101K-T	4	10		C	A
	2830 6229	Mylar capacitor	MAZV-104K50-T	2	10		C	A
	2830 6339	Mylar capacitor	AMZV-222K50-T	1	10		C	A
	2830 6436	Mylar capacitor	AMZV-473K50-T	1	10		C	A
O*	2830 6517	Mylar capacitor	AMZV-122K50-T	1	10		C	A
	2845 0280	Ferrite beads	EXC-ELDR35C	9	20		C	A
	3013 0175	SB coil	STB-060	1			C	B
	3025 0161	Filter	AL 305	1			C	B

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	3025 0203	EMI filter	EXC-EMT222DC	5			C	A
O*	3121 6063	Relay	G2VN-234PL	2			A	C
	3412 0441	Slide switch	SSSU14	1			B	B
O*	3500 3398	Pin assembly 3P	IL-G-3P-S3L2-E	2			X	A
	3500 3509	11P connector	IL-G-11P-S3L2-E	1			X	A
	3500 3622	Pin assembly 15P	IL-G-15P-S3L2-E	1			X	A
	3500 3975	Pin assembly 5P	IL-G-5P-S3L2-E	1			X	A
	3612 0789	Jack	YKB21-5010	10			X	A
O*	4307 9282	Blank PCB M5306-MA2M	M110256B-1	1			X	D
	3) M5306-MA5M PCB ASS'Y							
	2114 0021	Monolithic IC	LA6462D	1			A	B
	2114 0224	Monolithic IC	M5201P	1			A	B
	2220 1387	Transistor	2SC1740SQ-TP-T	1	10		A	A
	2607 5182	Carbon film resistor	ELR50X-8.2-J-T34VT	2	20		C	A
	2617 0028	Carbon film resistor	R-20-100-J-T24-T	2	20		C	A
	2617 0052	Carbon film resistor	R-20-1K-J-T24-T	2	20		C	A
	2617 0095	Carbon film resistor	R-20-10K-J-T24-T	7	20		C	A
	2617 0117	Carbon film resistor	R-20-47K-J-T24-T	2	20		C	A
	2617 0141	Carbon film resistor	R-20-100K-J-T24-T	2	20		C	A
	2617 0203	Carbon film resistor	R-20-470K-J-T24-T	2	20		C	A
	2617 0265	Carbon film resistor	R-20-10-J-T24-T	2	20		C	A
	2617 0491	Carbon film resistor	R-20-330K-J-T24-T	1	20		C	A
O*	2801 8680	Electrolytic capacitor	6.3RA2-33-T2-T	1	10		C	A
O*	2801 8743	Electrolytic capacitor	25RA2-47-T2-T	2	10		C	A
	2807 0276	Electrolytic capacitor	50RNBBP1-T2-T	5	10		C	A
	2818 0365	Ceramic capacitor	RT-HE50TKYB102K-T	1	10		C	A
	2818 0390	Ceramic capacitor	RT-HE40TKYB221K-T	1	10		C	A
	2818 1132	Ceramic capacitor	RT-HE40TKSL220K-T	1	10		C	A
	2830 6229	Mylar capacitor	AMZV-104K50-T	2	10		C	A
	2830 6237	Mylar capacitor	AMZV-102K50-T	1	10		C	A
	2845 0280	Ferrite beads	EXC-ELDR35C	1	20		C	A
	3013 0175	SB coil	STB-060	1			C	B
	3025 0203	EMI filter	EXC-EMT222DC	2			C	A
	3500 3401	Connector 4P	IL-G-4P-S3T2-E	1			X	A
	3501 3038	11P connector M306A	IL-11P-40-M306	1			X	B
	3612 0584	Jack	YKB21-5012	1			C	B
	3612 0789	Jack	YKB21-5010	1			C	B
	3613 0154	Jack	HLJ4406-01-3030	1			C	C
O*	4307 9352	Blank PCB M5306-MA5M	M110256B-2	1			X	A
	4) M5307-MA6M PCB ASS'Y							
O*	2010 6979	LSI	MB89352	1			A	R
	2105 1015	C MOS IC	TC74HC245AP	2			A	B
	2105 1099	C MOS IC	TC74HC32AP	1			A	B
O*	2105 1218	C MOS IC	TC74HC08AP	1			A	A
O*	2105 1260	C MOS IC	TC74HCU04AP	1			A	A
O*	2590 0581	Crystal oscillator	NR-18-8.00MHZ	1			A	B
	2617 0028	Carbon film resistor	R-20-100-J-T24-T	4	20		C	A
	2617 0036	Carbon film resistor	R-20-220-J-T24-T	18	20		C	A
	2617 0176	Carbon film resistor	R-20-1M-J-T24-T	1	20		C	A
	2617 0273	Carbon film resistor	R-20-22-J-T24-T	25	20		C	A
	2617 0386	Carbon film resistor	R-20-330-J-T24-T	18	20		C	A
O*	2801 8722	Electrolytic capacitor	6.3RA2-100-T2-T	1			C	A
O*	2801 8750	Electrolytic capacitor	6.3RA2-470-T2-T	1			C	A
	2818 2082	Ceramic capacitor	RT-HE70TKYF103Z-T	8	10		C	A
	2818 3275	Ceramic capacitor	RT-HE40TKCH220J-T	6	10		C	A

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	2845 0280	Ferrite beads	EXC-ELDR35C	1	20		C	A
	3025 0203	EMI filter	EXC-EMT222DC	8			C	A
O*	3025 0406	EMI filter	ELX-TV150GA-T	18			C	A
	3501 1078	D sub connector	DBLC-J25SAF-10L6	1			X	C
O*	3501 3675	Header	7630-5002FL	1			X	B
O*	3501 3682	4P connector M307D	IL-4P-70-M307	1			X	B
O*	4317 0380	Blank PCB M5307-MA6M	M110453-1	1			X	H
	5) M5306-PS1M PCB ASS'Y							
	2114 0231	Monolithic IC	AN78M05R	1			A	B
	2114 0238	Monolithic IC	M5230L	1			A	B
	2114 0245	Monolithic IC	M51954BL	1			A	B
	2121 0013	OP amp	NJM4558DD	1			A	B
	2121 0072	Monolithic IC	NJM2068DD	1			A	B
	2200 4409	Transistor	2SA933-SQ-TP-T	2	10		A	A
	2220 1387	Transistor	2SC1740SQ-TP-T	7	10		A	A
	2230 1373	Transistor	2SD400E,F	2	10		A	A
	2230 5229	Transistor	2SD1666R,S	1			A	B
	2251 0245	Transistor	2SB891Q,R	1			A	A
	2253 0154	Transistor	2SD1381Q,R	1			A	A
	2300 9200	Diode stack	S2VB10-4009(F03)	1			B	B
	2301 0241	Diode	1SS254T-77-T	2	20		C	A
	2360 0378	Zener diode	RD13ESB2-T1-T	1	20		B	A
	2360 0385	Zener diode	RD4.7ESB1-T1-T	3	20		B	A
	2390 0217	Diode stack	S1WBA10-4001	1	5		B	B
	2390 0294	Diode stack	S1YB10-4001	1	5		B	B
	2390 0378	Diode	1SR139-100T-32-T	4	20		C	A
	2390 0658	Diode stack	D5FB10-4003(L10)	1			B	C
	2605 0287	Metal film resistor	CRH100FH11-J-0.68	1	20		C	A
	2605 0427	Metal film resistor	CRH100FH11-J-18	1	20		C	A
	2605 0434	Metal film resistor	CRH100FH-J-39	2	20		C	A
	2608 0042	Carbon film resistor	F-25-1M-J-FH04	1	20		C	A
	2606 0315	Carbon film resistor	R-20-3.3-J-T24-T	2	20		C	A
	2606 0504	Carbon film resistor	R-20-24K-J-T24-T	1	20		C	A
	2606 0539	Carbon film resistor	R-20-1.8-J-T24-T	1	20		C	A
	2607 5084	Carbon film resistor	ELR50X-1-J-T34V-T	3	20		C	A
	2607 5091	Carbon film resistor	ELR50X-1.5-J-T34VT	2	20		C	A
	2607 5147	Carbon film resistor	ELR50X680-J-T34-T	1	20		C	A
	2607 5154	Carbon film resistor	ELR50X470-J-T34-T	1	20		C	A
	2617 0028	Carbon film resistor	R-20-100-J-T24-T	1	20		C	A
	2617 0044	Carbon film resistor	R-20-560-J-T24-T	4	20		C	A
	2617 0061	Carbon film resistor	R-20-2.2K-J-T24-T	1	20		C	A
	2617 0079	Carbon film resistor	R-20-3.3K-J-T24-T	1	20		C	A
	2617 0095	Carbon film resistor	R-20-10K-J-T24-T	4	20		C	A
	2617 0231	Carbon film resistor	R-20-270-J-T24-T	1	20		C	A
	2617 0246	Carbon film resistor	R-20-12K-J-T24-T	1	20		C	A
	2617 0265	Carbon film resistor	R-20-10-J-T24-T	4	20		C	A
	2617 0289	Carbon film resistor	R-20-15K-J-T24-T	2	20		C	A
	2617 0360	Carbon film resistor	R-20-1.5K-J-T24-T	1	20		C	A
	2617 0378	Carbon film resistor	R-20-3.9K-J-T24-T	2	20		C	A
	2617 0505	Carbon film resistor	R-20-33-J-T24-T	1	20		C	A
	2617 0877	Carbon film resistor	R-20-8.2K-J-T24-T	1	20		C	A
	2760 2207	Semi fixed resistor	V8K4-11B2K	3	10		B	A
	2801 7910	Electrolytic capacitor	16RE3-470-T2-T	1	10		C	A
	2801 8127	Electrolytic capacitor	6.3RE3-1000-T2-T	1	10		C	A
O*	2801 8505	Electrolytic capacitor	50RA2-4R7-T2-T	1	10		C	A
O*	2801 8694	Electrolytic capacitor	16RA2-100-T2-T	2	10		C	A

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O*	2801 8722	Electrolytic capacitor	6.3RA2-100-T2-T	1	10		C	A
O*	2801 8736	Electrolytic capacitor	16RA2-10-T2-T	1	10		C	A
O*	2801 8743	Electrolytic capacitor	25RA2-47-T2-T	2	10		C	A
O*	2801 8750	Electrolytic capacitor	6.3RA2-470-T2-T	3	10		C	A
O*	2801 8757	Electrolytic capacitor	16RA2-22-T2-T	3	10		C	A
O*	2801 8764	Electrolytic capacitor	25RA2-22-T2-T	2	10		C	A
O*	2801 8771	Electrolytic capacitor	25RA2-220-T2-T	1	10		C	A
O*	2801 8778	Electrolytic capacitor	50RA2-1-T2-T	2	10		C	A
	2801 7224	Electrolytic capacitor	16RP2-10000	1			C	C
	2801 7980	Electrolytic capacitor	35LP3-2200	1			C	B
O*	2801 8785	Electrolytic capacitor	25RA2-1000	1			C	B
O*	2801 8792	Electrolytic capacitor	35RA2-1000	1			C	B
O*	2813 0756	SC capacitor	DD306F104Z25-T	2	10		C	A
	2818 0446	Ceramic capacitor	RT-HE40TKYB101K-T	2	10		C	A
	2818 2082	Ceramic capacitor	RT-HE70TKYF103Z-T	2	10		C	A
	2818 2601	Ceramic capacitor	DE7150FZ103PVA1	2	5		C	B
	2830 6229	Mylar capacitor	AMZV-104K50-T	4	10		C	A
	2830 6270	Mylar capacitor	AMZV-223K50-T	1	10		C	A
	2831 0280	Mylar capacitor	AMZV-334K-50	1			C	C
	3020 2104	Noise filter	TF2317C-601Y2R5	1			C	B
	3025 0203	EMI filter	EXC-EMT222DC	1			C	A
	3501 0917	PCB connector	B2P3-VH	1			X	A
	3501 2884	PCB connector	B8P9S-VB	1			X	A
	3501 3045	5P connector M306A	IL-5P-38-M306	1			X	B
	3501 3052	4P connector M306C	AMPEI-4P-24-M306	1			X	B
	3501 3059	10P connector M306A	I1-10P-41-M306	1			X	B
	3501 3066	2P connector M306A	I1-2P-19-M306	1			X	A
	3613 0217	Receptacle	NC-174-10-C	1			X	B
	3841 1217	Booster	E1-M172A	1			C	C
O*	4307 9343	Blank PCB M5306-PS1M	M110258C-1	1			X	D
	6) M5306-CN1M PCB ASS'Y							
	2301 0101	Diode	1S2473-T-77-T	24	20		C	A
	2614 0170	Carbon film resistor	R-25-330-J-T24-T	5	20		C	A
	2370 0035	LED	LN851RPP.WE	5	20		B	A
	3410 1728	Tact switch	EVQ-QS205K	24	10		B	A
	3725 1295	PC joiner M306B	CUJ-UL-19-190	1			C	B
	4307 9290	Blank PCB M5306-CN1M	M110257-1	1			X	C
	4307 9300	Blank PCB M5306-CN2M	M110257-2	1			X	A
	4307 9310	Blank PCB M5306-CN3M	M110257-3	1			X	A
	7) M5306-CN4M PCB ASS'Y							
	2614 0145	Carbon film resistor	R-25-100-J-T24-T	2	20		C	A
	2770 9672	Slide VR	EWA-NFO-C10-B14	1			B	B
	2770 9681	Slide VR	EWA-NFO-C10-B54	1			B	B
	3501 3017	3P connector M306A	IL-3P-19-M306	1			X	A
	3501 3024	4P connector M306A	IL-4P-13-M306	1			X	B
	4307 9320	Blank PCB M5306-CN4M	M110257-4	1			X	A
	8) M5306-CN5M PCB ASS'Y							
	2614 0145	Carbon film resistor	R-25-100-J-T24-T	1	20		C	A
	2770 9681	Slide VR	EWA-NFO-C10-B54	1			B	B
	3501 3031	4P connector M306B	IL-4P-17-M306	1			X	B
	4307 9330	Blank PCB M5306-CN5M	M110257-5	1			X	A

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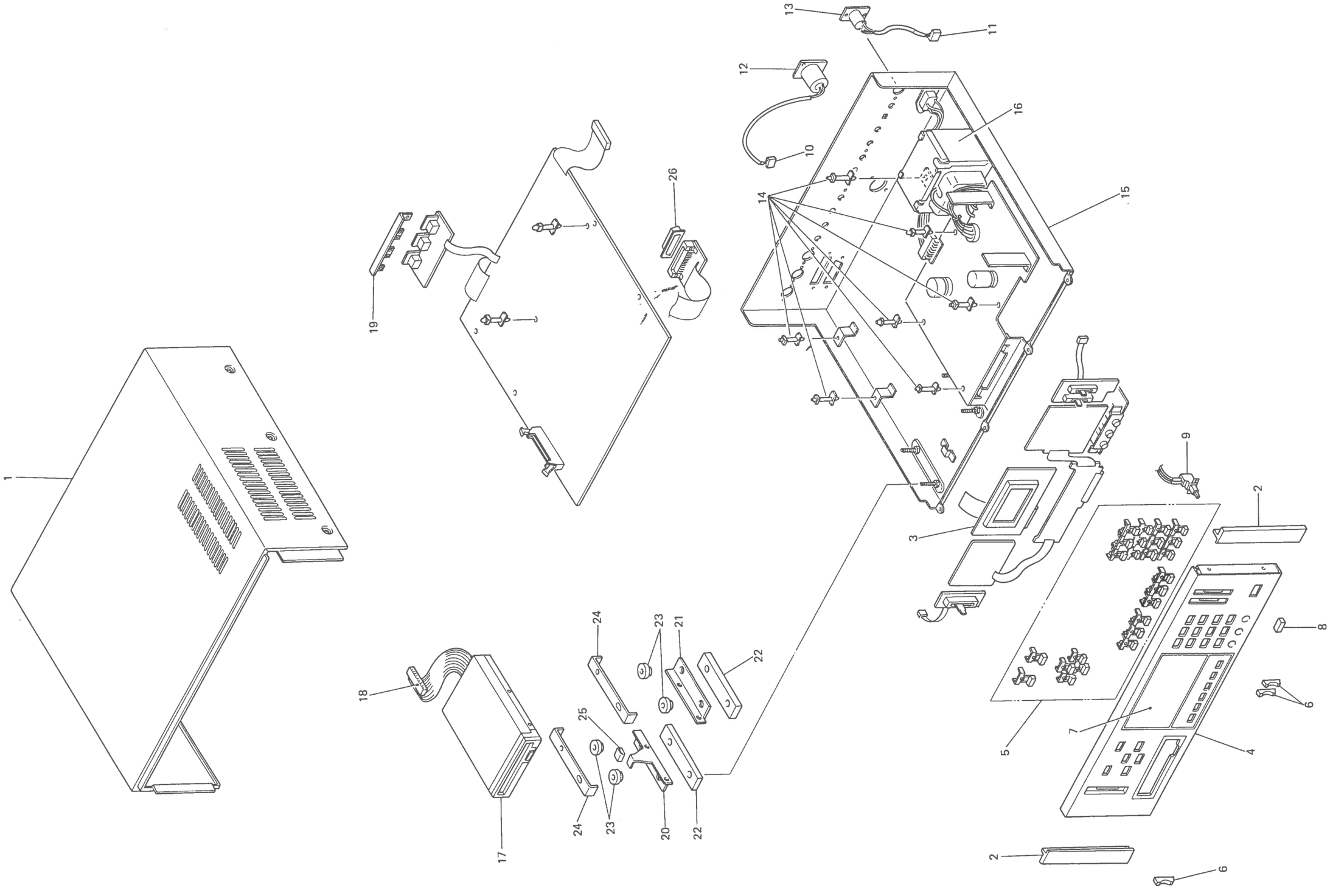
		9) POWER ASS'Y						
	2251 0098	Transistor	2SB942Q,R	1			A	B
	2253 0084	Transistor	2SD1267Q,R	1			A	B
	2253 0140	Transistor	2SD1488Q,P	2			A	C
	3012 0252	Power transformer	TE-306-1M1	1			B	U
O*	6914 4780	Heat sink holder (L)	M410250-1	1			X	A
O*	6914 4790	Heat sink holder (R)	M410251-1	1			X	A
O*	6914 6021	Heat sink 306	M310283A-1	1			X	K
		10) FRONT CHASSIS UNIT						
	3335 1547	LCD module	DMF668N-EB2	1			A	AA
	3440 5328	Power switch	SDLC-1P-011	1			A	B
O*	3501 3654	2P connector M307C	VHR-2P-27-M307	1			X	B
	6913 9740	PW knob	M41093-12	1			C	A
O*	6912 7693	Front chassis sub ass'y	M210223C*3	1			C	R
	6914 4540	Key top set 306	M310357*1	1			C	C
	6914 4550	Slide knob 306	M310277-1	3			C	A
	6914 4561	Panel 306	M310279A-1	1			C	E
	6914 4450	Side panel 306	M310282-1	2			C	H
O*	6914 8870	Panel sheet	M410475-1	1			C	A
		11) LOWER CASE UNIT						
O*	1012 8582	FDD	JU-255-1P	1			A	DD
	3501 3073	34P connector M306A	7934-34P-18-M306	1			X	D
O*	3501 3647	30P connector M307A	7930-30P-18-M307	1			X	C
O*	5860 1589	Card spacer	KGLS-18S	9			X	A
	6904 6140	DIN jack holder 153	M31619-1	1			X	A
	6914 4460	FDD angle (L)	M410252-1	1			X	B
	6914 4470	FDD angle (R)	M410253-1	1			X	B
	6914 4480	FDD chusion A	M410254-1	2			X	B
	6914 4490	FDD chusion B	M410255-1	4			X	A
	6914 4500	FDD rating plate 306	M410260-1	2			X	B
	6914 4510	PCB damper 306	M410261-1	1			X	A
O*	3501 3199	3P connector M306B	IL-3P-26-M306	1			X	B
O*	3501 3206	3P connector M306C	IL-3P-10-M306	1			X	B
	3613 0483	Jack	XLR-3-31	1			B	I
	3613 0490	Jack	XLR-3-32	1			B	F
O*	6912 7683	Lower case sub ass'y	M210224C*2	1			C	T
		12-a) OTHERS						
	5860 1379	Dust cap	025-5057-000-1	2			C	A
	6914 4440	Upper case 306	M110170-1	1			X	C
		12-b) OTHERS						
O*	1012 8365	Flopy disk	FL-D1	1			C	L
O*	1012 8372	Flopy disk	FL-D2	1			C	L
	3700 9491	Cord set	6.3MPP-L300-H-9	1			C	E
	3719 1400	MIDI cable	HD-D5P-0003	1			C	K
	3501 2513	PCB connector	B2P(4-2,3)-VH	1			X	A
	3600 1186	Voltage selector	ESE-371	1			C	B
	3631 0049	UL time lug fuse	UL-TSC-1A	2	10		A	A
	3631 0081	UL time lug fuse	UL-TSC-1.6A	1	10		A	A
	3631 0138	UL fuse	UL-TSC-2.5A	1	10		A	A
	3631 2017	UL time lug fuse	MT4-1.5A	1			A	B
	3700 3051	Cord set	UC-907-J01	1			C	D
O*	6916 3530	Rating label	M410757-7	1			C	A
O*	6916 3540	Rating plate	M41669-39	1			C	A

Notes: O* – New parts
Q'ty – Quantity used per unit
* – Minimum order and supply quantity

Rank A: Essential
B: Stock recommended
C: Others
X: No stock recommended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FLOPPY DISK DRIVE UNIT

JU-255-P

PART. 1

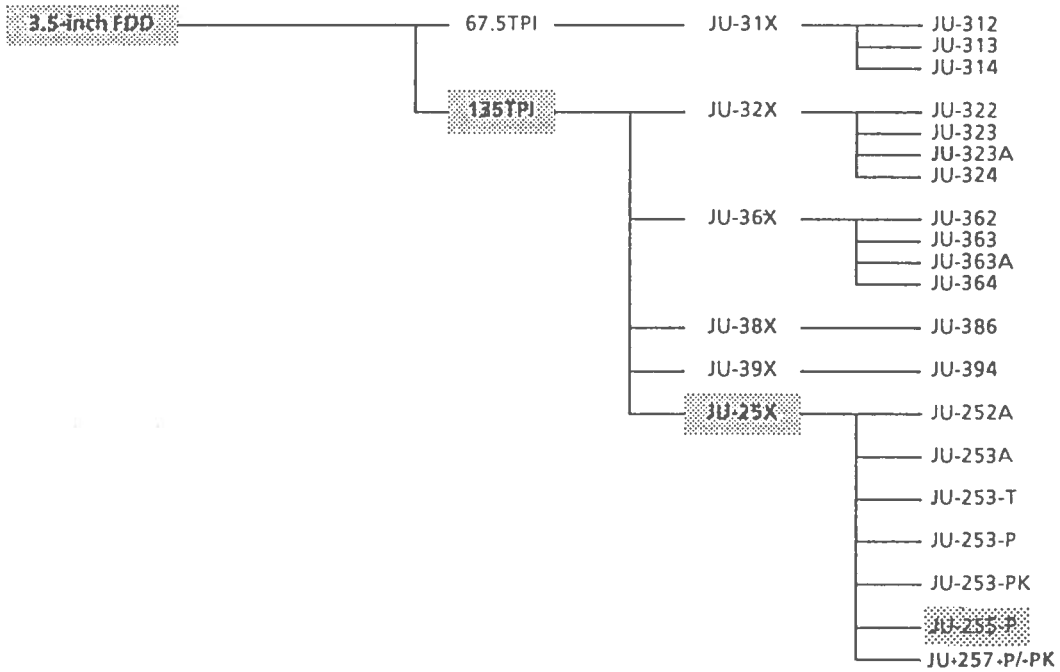
1. INTRODUCTION

This service manual consists of two parts. Part 1 covers maintenance description, adjustment procedures, and trouble analysis and Part 2 covers disassembly and reassembly procedures, parts list, and PCB circuits. Refer to the highlighted applicable items, and perform maintenance work on the Floppy Disk Drive (FDD).

Note :
This service manual is prepared for maintenace of the Floppy Disk Drive.
Do not use this manual for judging pass or fail criteria in inspections.

2. MODELS AND MODEL NUMBERS

2.1 3.5-inch FDD Series



3. SPECIAL TOOLS

The following special tools are used for FDD maintenance.

TABLE 3.1

Tool		P/No.				Quantity
		JU-253-T/-P/-PK	JU-257-P/-PK	JU-252A JU-253A	JU-31X,32X,36X, JU-323A,363A	
Exerciser		YTFD-EXT-35	* ←	* ←	* ←	1
Alignment Diskette	DAD	JU-01AA	817-384	JU-01AA	* ←	1~2
	CE	817-363CE		* ←	* ←	
Data Diskette		2DD	2DD/2HD	2DD	* ←	1~2
CMOS/TTL Adaptor		YTFDD-CN35	* ←	* ←	* ←	1
Step Motor and Head Assy Mounting Jig		NOT required	* ←	* ←	YTFDD-SB35	1
Test Pin Jig For PCB			YTFD-TPIN25X	YTFDD-TPIN25	YTFDD-TPIN35	1
DAD Alignment Tester		JU-02A	* ←	* ←	* ←	1
Oscilloscope (50MHz)						1
Probe (10:1)						3
Frequency Counter						1

Note: * ← : Stand for the same as left.
DAD : Dynamic Alignment Diskette
CE : Cats Eye

4. OUTLINE OF MAINTENANCE

• The following tools are required for maintenance of a Floppy Disk Drive.

4.1 Alignment Diskette

Alignment diskette is used for head actuator alignment and index sensor adjustment. Use the right diskette as shown in Table 3.1.

4.2 Exerciser

The exerciser enables you to make all adjustments and inspections necessary for an FDD. Its functions include the following:

(1) Seek increment or alternate tracks
(2) Read (but no data compare)
(3) Write 1F or 2F (All 0's or 1's)
(4) Recalibration to track 00

The exerciser has switches and indicators to execute a specified function.

5. DIAGNOSTIC PROCEDURES

5.1 Error Symptom Recognition

Errors that occur because of the wrong operating procedure, wrong programming, or use of a defective diskette, or soft errors due to external causes, such as contaminated air and random electrical noise, are often attributed to a drive failure.
Unless a visual inspection of the drive reveals an evident assembly fault or a defect, **always confirm errors with another good diskette, and another known good drive.**

5.2 Soft Error Detection and Correction

Soft errors are normally caused by the following:

(1) Contamination between read/write heads and diskette. This kind of contamination can be easily eliminated by the liner in the diskette. Contaminated heads can be cleaned by a general purpose non-abrasive head cleaning diskette. Please follow the suitable procedure provided with the cleaning diskette.
(2) Random electrical noise, normally a few microseconds or less.
(3) Small defects in written data and/or track not detected during write operation may cause soft errors during read.
(4) Faulty grounding of the drive or host system can also cause a soft error.
(5) Wrong motor speed is another cause of soft errors.

Take the following steps on the controller side to recover from the soft errors mentioned above.

(1) Read the track again ten times or until the data is recovered.
(2) If Step (1) above fails to recover the data, access the adjacent track. Then return the head to the original track.
(3) Repeat Step (1).
(4) Any error that cannot be corrected by the above procedure is irrecoverable.

5.3 Write Error

If an error occurs during write operation, it is usually detected during the next revolution by performing a read operation called write check. To correct an error, write again and repeat a write check operation. If the result is unsatisfactory after ten or more write operations, perform a read operation on another track to determine whether it is the diskette or the drive that is wrong. If an error persists, replace the diskette and repeat the above procedure. If the error still persists, consider the drive defective. If the error is corrected, dispose of the diskette as defective.

5.4 Read Error

Most read errors are soft errors. Data can be recovered by following the recovery procedure mentioned in 5.2.

5.5 Seek Error

(1) Stepper motor or stepper motor drive circuit is faulty.
(2) Faulty carriage
There are two ways of seek error recovery. One is to recalibrate to track 00 , and seek back to the original track. The other is to read the ID field, check the track number on which the head is located, and move the head away from it. And read it again.

5.6 Interchangeability Error

Data which is written by one drive may not be read by another. This error is called a Interchange-ability error,which can be caused mostly by the following reason,which should be checked as follows.

(1) Head misalignment: Refer to Adjustments and Confirmation Item 9.6
(2) Head output too low: Refer to Adjustments and Confirmation Item 9.3
(3) Motor speed difference: Refer to Adjustments and Confirmation Item 9.1
(4) Format difference

6. TROUBLE ANALYSIS

To determine the cause of trouble whether it lies in the FDD, diskette, or controller, replace the disk and FDD with good ones. If the FDD is assumed faulty as a result, follow the procedure below.

6.1 Trouble Analysis Procedure

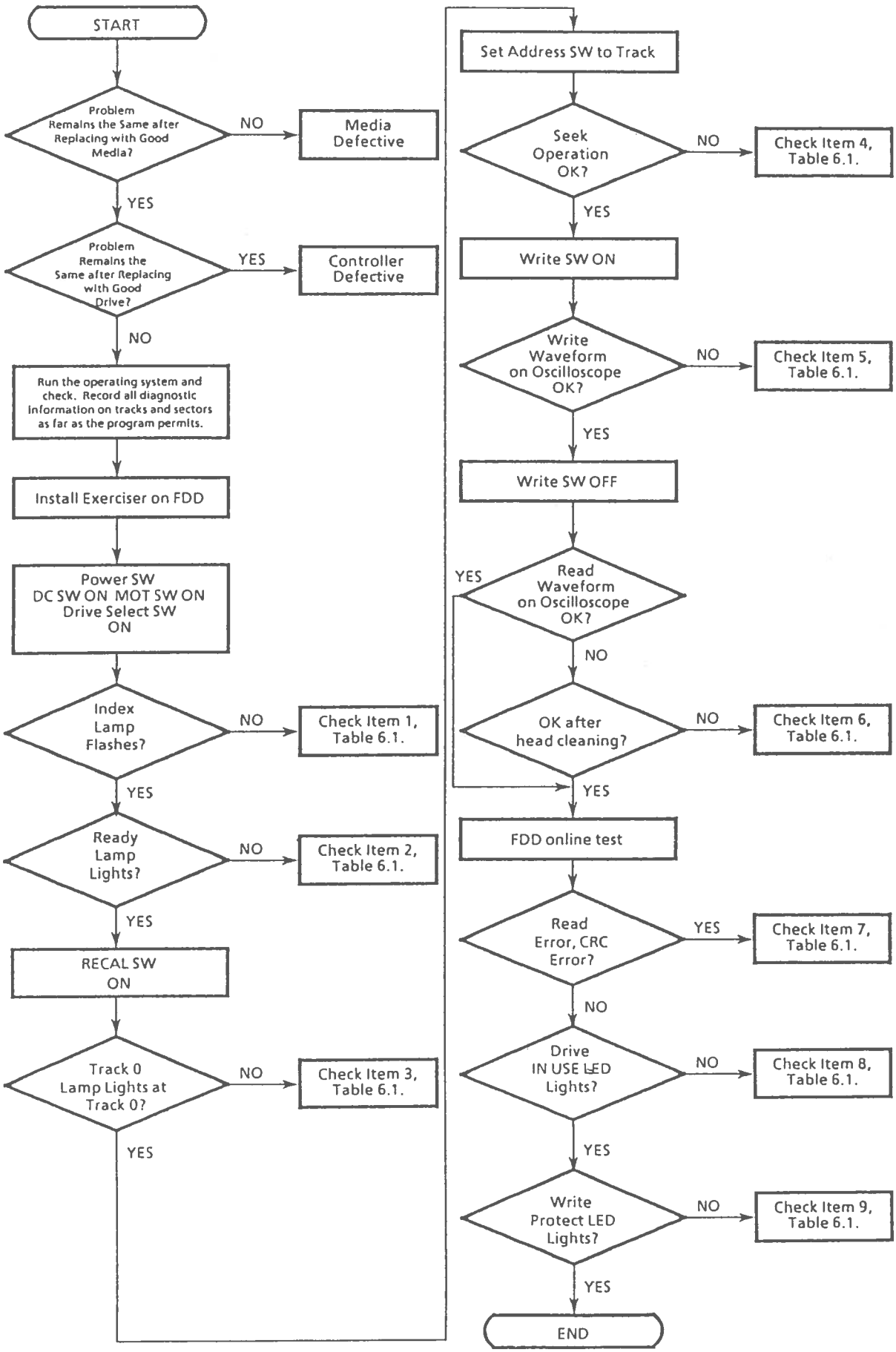
FDD trouble may occur in any of the following nine forms.
(1) Index detection failure
(2) Not ready
(3) Track 0 undetectable
(4) No seek
(5) No write
(6) No read
(7) Read error
(8) IN USE LED won't light.
(9) Write protect undetectable

Check with the troubleshooting flowchart in 6.2

CAUTION:

Be sure to switch power off before removing an FDD or PCB from the operating system.

6.2 Trouble Shooting Flow Chart



6.3 Trouble Analysis Table

Table 6.1

Item	Trouble	NO	Cause	JU-3X3, 3X4, 323A, 363A, 38X, 39X	JU-3X2, 252A, 253A, 253-T, 253-P/-PK
1	Index detection failure	1	DD motor control PCB	Replace DD motor, Base assembly	Replace DD motor assembly
		2	DD motor faulty		
		3	Index LED faulty	Replace DD motor, Base assembly	Replace
		4	Index detector faulty		
		5	PCB motor ON circuit	Repair	* ←
		6	PCB index detection circuit	Repair	* ←
2	Not ready	1	See Item 1.		
		2	PCB ready circuit	Repair	* ←
3	Track 0 detection failure	1	Track 00 assembly	Replace	* ←
		2	PCB track 0 detection failure	Repair	* ←
4	No seek	1	Stepper motor	Replace	* ←
		2	Guide shaft contamination or damaged	Replace	* ←
		3	PCB stepper driver circuit	Repair	* ←
5	No WRITE	1	See Item 1.		
		2	Head disconnected	Replace	* ←
		3	Head shorted	Replace	* ←
		4	PCB write circuit	Repair	* ←
6	No READ	1	See Item 1.		
		2	See Item 5.		
		3	PCB read circuit	Repair	* ←
7	READ ERROR	1	See Item 1.		
		2	See Item 6.		
		3	Alignment	Adjustable.	* ←
		4	Azimuth	Unadjustable	* ←
		5	Burst	Unadjustable	Adjustable
		6	Asymmetry	Adjustable	* ←
		7	Limiter	Adjustable	
		8	Flag 0	Adjustable	* ←
		9	Index period	Replace DD motor, Base assembly	Replace DD motor assembly
		10	PCB read circuit	Repair	* ←
8	IN USE LED won't light.	1	LED part	Repair	* ←
		2	PCB IN USE circuit	Repair	* ←
9	Write protect failure	1	Write protect part	Replace DD motor, Base assembly	Replace
		2	Write protect circuit	Repair	* ←

Note: * ←: Stand for the same as left.

6.4 Adjustment Procedures on Replacement of the Head Assembly and Control Board Assembly of the JU-257-P (excluding-PF)

Each of the Head Assembly and Control Board Assembly of the JU-257-P has four ranks (A to D), so be sure to use a pair of these assemblies of the same rank.

[Replacement Procedure]

(1) Replacement of the Head Assembly
1. Confirm the rank of the new head assembly to be mounted. (Refer to Figure 6.1 Rank Marking.)
2. Replace three resistors (R19, R20, and R44) on the control board assembly in reference with the rank table below so that the rank of the assembly becomes the same as that of the head assembly confirmed in step 1 above.

(2) Replacement of the Control Board Assembly
1. Confirm the rank of the currently mounted head assembly.
2. Replace three resistors (R19, R20, and R44) on the control board assembly in reference with the rank table in table 6.2 so that the rank of the assembly becomes the same as that of the head assembly confirmed in step 1 above.

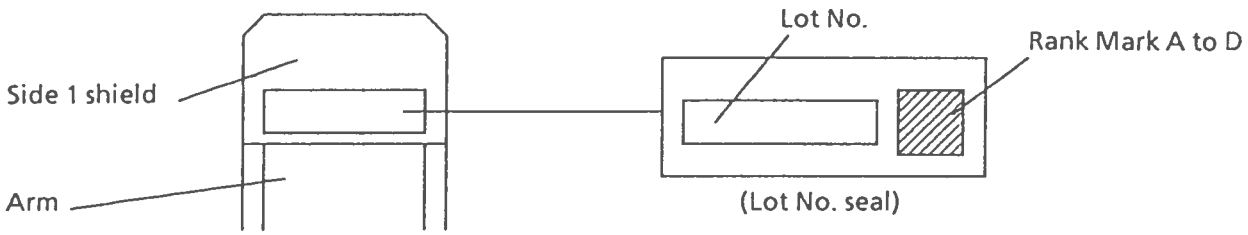


Fig. 6.1 Head Assembly Rank Marking Position

Table 6.2 Resistances on the Control Board

Resistor / Head ass'y rank	Circuit Ref. No.	Resistance	Part No.
A	R19	1.8 kΩ	MCR18EZHJ182
	R20	15.6 kΩ	MCR18EZHJ562
	R44	680 Ω	MCR18EZHJ681
B	R19	2.7 kΩ	MCR18EZHJ272
	R20	9.1 kΩ	MCR18EZHJ912
	R44	1.2 kΩ	MCR18EZHJ122
C	R19	3.9 kΩ	MCR18EZHJ392
	R20	9.1 kΩ	MCR18EZHJ912
	R44	1.5 kΩ	MCR18EZHJ152
D	R19	3.9 kΩ	MCR18EZHJ392
	R20	9.1 kΩ	MCR18EZHJ912
	R44	1.5 kΩ	MCR18EZHJ152

7. PREVENTIVE MAINTENANCE

No preventive maintenance is necessary for any type of FDDs under normal conditions of use.
However if it is determined that adjustments are necessary,the following must be done.

- Adjustments (Refer to table 8.1)

(1) Make a read/write head radial adjustment at a specified track. (Sides 0,1)
(2) Make an index timing adjustment at a specified track. (Sides 0,1)
(3) Make an azimuth measurement at a specified track. (Sides 0,1)

CAUTION

Do not write when using alignment diskette. Check that write protect sensor is properly operating with a data diskette.

Note : Section 9 describes the adjustment procedures in detail.

8. MEASUREMENT ITEMS

Table 8.1

Item	Parameter	JU-252A, 253A		JU-253-T	
		TRK	Value	TRK	Value
1	Index period	40	200 ± 2 ms	40	200 ± 2 ms
2	Output level	79	80 mV or more	79	80 mV or more
3	Modulation	0, 79	20% or less	0, 79	20% or less
4	Resolution	79	55% or more	79	55% or more
5	Radial Alignment	40	± 25µm	40	± 25µm
	Reference (DAD)		(43% or more)		(43% or more)
	Reference (CE by 817-363CE)		(55% or more)		(55% or more)
6	Azimuth	40	± 24'	40	± 24'
7	Index burst	40	3 ± 1.7 ms	40	3.1 ± 0.4 ms
8	Flag 0	From track 0 to track 1 and back	TR00 (TR0 : Low, TR1 : High)	From track 0 to track 2 and back	1 : 1
9	Asymmetry	79	≦ 700 ns	79	≦ 700 ns

Item	Parameter	JU-257-P/-PF		
		TRK	Value (257-P)	Value (257-PF)
1	Index period	40	200 ± 3 ms	200 ± 3 ms
2	Output level	79	2.0M :50mv or more 1.0M : 90mV or more	2.0M : 50mV or more 1.0M : 120mV or more
3	Modulation	0, 79	20% or less	20% or less
4	Resolution	79	2.0M : 63% or more 1.0M : 60% or more	2.0M : 63% or more 1.0M : 55% or more
5	Radial Alignment	40	± 25µm	± 25µm
	Reference (DAD)		(43% or more)	(43% or more)
	Reference (CE by 817-363CE)		(55% or more)	(55% or more)
6	Azimuth	40	± 18'	± 18'
7	Index burst	40	3.1 ± 0.4 ms	3.1 ± 0.4 ms
8	Flag 0	From track 0 to track 2 and back	1 : 1	1 : 1
9	Asymmetry	79	2.0M : ≦ 350ns 1.0M : ≦ 700ns	2.0M : ≦ 350ns 1.0M : ≦ 700ns

9. ADJUSTMENTS AND VERIFICATIONS

9.1 Motor Speed Verification (Index Period)

(1) Insert a diskette, run the motor, and clamp. Refer to the index period column of Table 8.1 for the applicable model.
(2) Step to the specified track.
(3) Connect a frequency counter to the INDEX signal.
Index (No. 8 Pin of CMOS/TTL Adaptor)
(4) Check that the frequency counter readings meet the specifications in the table.

9.2 Write Protect Verification

(1) Check that the exerciser's write protect lamp goes on and off as a media is inserted and removed as specified in the table below.

Media with write protect hole open	:	ON	(Write protected)
Media with write protect hole closed	:	OFF	(Not write protected)

9.3 Head Output Verification

Use a new diskette if possible to identify head failure for this check.

(1) Insert a good diskette.
(2) Run the motor.
(3) Step to the track specified in the output level column of Table 8.1.
(4) Connect the oscilloscope probe as specified below.

CH1 : T1
CH2 : T2
EXT: Index (No. 8 Pin of CMOS/TTL Adaptor)

Invert channel 2 and select the Add mode.
Set vertical deflection to 10 mV/division and horizontal deflection to 20 ms/division.
(5) Write 2F (all ones) on the entire circumference.
(In case of a double-sided FDD, repeat it on sides 0 and 1 using SIDE SELECT.)
(6) Check that the average output level meets the specifications of Table 8.1.

$$\left[V \text{ average} = \frac{Vmax + Vmin}{2} \right]$$

If it does not meet the specifications, refer to Item 7 of the Trouble Analysis Table.

9.4 Output Modulation Verification

Modulation: M is calculated by the following formula.

$$M(\%) = \frac{Vmax - Vmin}{Vmax + Vmin} \times 100$$

using the value obtained in 9.3, and check that the calculated value meets the specifications of Table 8.1.

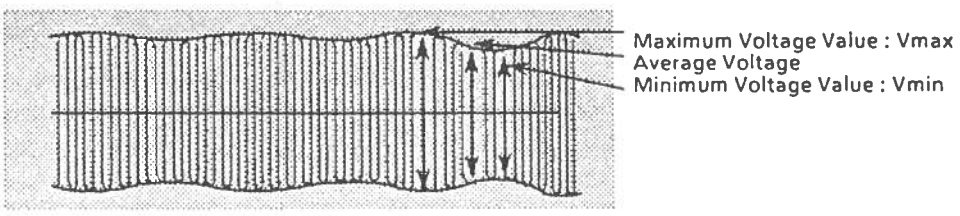


Fig. 9.1 Modulation

9.5 Resolution Verification

(1) Leave the oscilloscope in the same condition as mentioned in section 9.3.
(2) Resolution is calculated by the following formula.

$$\frac{V_{2F}\ \text{average}}{V_{1F}\ \text{average}} \times 100\ (\%)$$

(3) Check that the calculated value meets the specifications of Table 8.1.

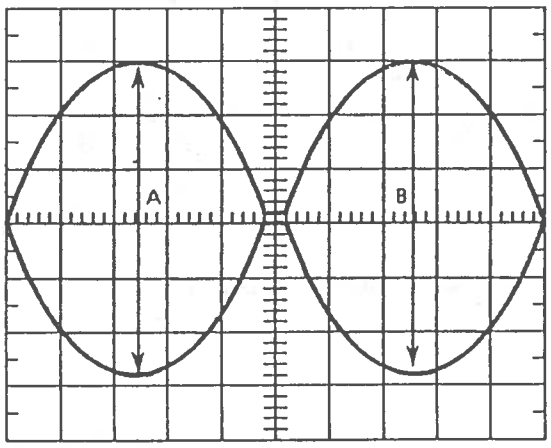
9.6 Radial Alignment Adjustment

Introduction
This adjustment is normally not necessary.
If the mounting screws for the stepper motor loosen, or if parts become defective, or if a compatibility error occurs, check and readjust according to the following procedure.
Steps (4) to (9) below should be performed regardless of the type, CE or DAD alignment diskette used. Use an alignment diskette suitable to the type of FDD to be adjusted according to table 3.1.

(1) Insert Panasonic alignment diskette.
CAUTION:
Be sure to leave the alignment diskette under room conditions for 20 minutes before adjustment.
(2) Step to the track specified in the Radial alignment column of Table 8.1.
(3) Leave the oscilloscope in the same condition as mentioned in section 9.3.

- Cats Eye System

(4) Check the output waveforms for sides 0 and 1. They should appear as in Fig. 9.2.
(5) The two waveforms should appear in the amplitude ratio in the R/A colum of Table 8.1 or better.
(6) If the specified ratio is not satisfied, loosen the two mounting screws for the stepper motor.
(7) Move the stepper motor along the base by hand until the two waveforms assume approximately the same amplitude, and retighten the mounting screws. (See Fig. 9.2.)
(8) Step the head outward (track 0) and inward (track 40 or 79), and confirm that the adjustment has been completed.
(9) After the radial adjustment, be sure to confirm track 00 sensor adjustment 9.9



$A > B \ : \ \frac{B}{A} \times 100$

$B > A \ : \ \frac{A}{B} \times 100$

Fig. 9.2 Radial Alignment Waveforms (CATS EYE)

Note: Alignments on sides 0 and 1 are adjusted at the factory. If they are misaligned, adjust them to meet the specifications of Table 8.1.

- DAD (Dynamic Alignment Diskette)

(4) Watch the output waveforms for sides 0 and 1. They should appear as shown in Fig. 9.3.
(5) Measure the timing levels A_1 to A_4 and B_1 to B_4 in Fig. 9.3, and calculate the lobe ratio from the following formulas.

$$\Sigma A > \Sigma B : \frac{\Sigma B}{\Sigma A} \times 100\% \qquad \Sigma A < \Sigma B : \frac{\Sigma A}{\Sigma B} \times 100\%$$

(6) The lobe ratio calculated by the above formulas should meet the specifications on item 3 of Table 8.1.
(7) If the above requirement is not met, loosen the two mounting screws for the stepper motor, adjust.
(8) Seek from track 0 to track 40 and from track 79 to track 40, and confirm that the adjustment has been completed.
(9) After the radial adjustment, be sure to confirm track 00 sensor adjustment 9.9.

Note: A digital alignment test instrument for 3.5-inch FDDs permits accurate and easy adjustment because the lobe ratio is displayed on the instrument.

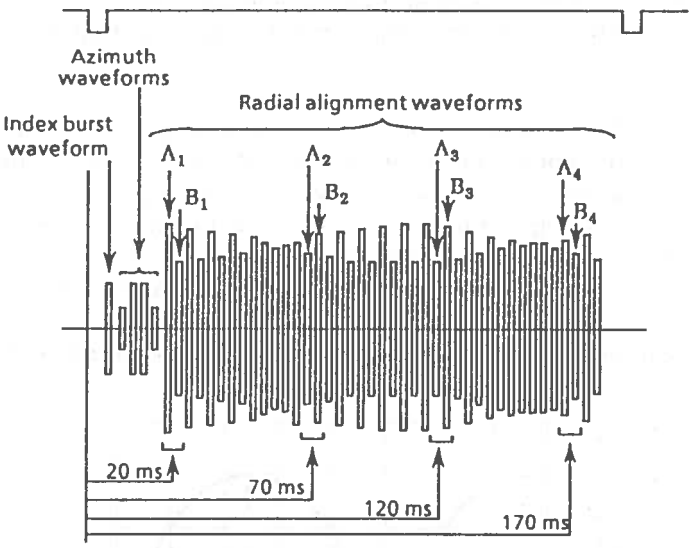


Fig. 9.3 Alignment Waveform (DAD)

9.7 Azimuth Verification

(1) Insert an alignment diskette. Seek to the track specified in the azimuth column of Table 8.1.
(2) Set the oscilloscope in the same conditions as in 9.3, and set horizontal deflection to 2ms/div (DAD) or 0.5 ms/div (CE).
(3) Measure as shown below.
(4) Confirm that the measured value meets the specifications in the azimuth column of Table 8.1.

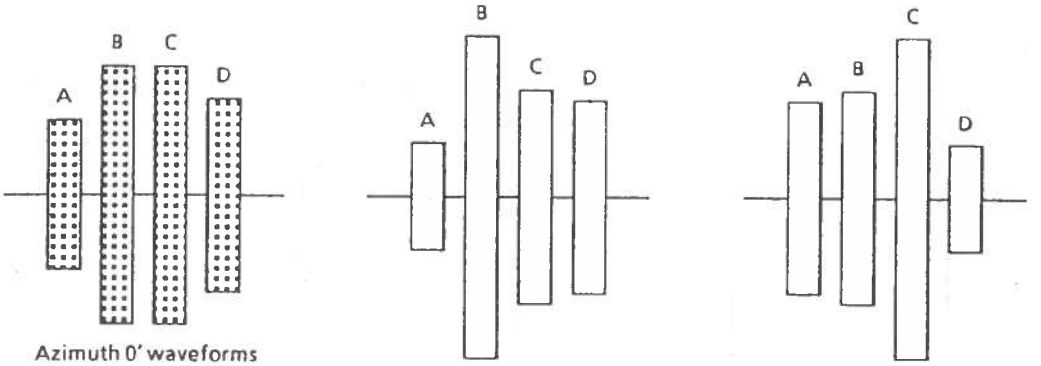


Fig. 9.4 Azimuth Waveforms

9.8 Index Burst Verification and Adjustment

(1) Insert an alignment diskette. Seek to the track specified in the I/B column of **Table 8.1.**
(2) Set the oscilloscope time base as follows:
1 ms/division
(3) Check that the time from oscilloscope start to the first data pulse meets the I/B specifications of Table 8.1. (DAD system)
(4) If Index Burst is not within specification, adjust the variable resister on the motor control PCB.

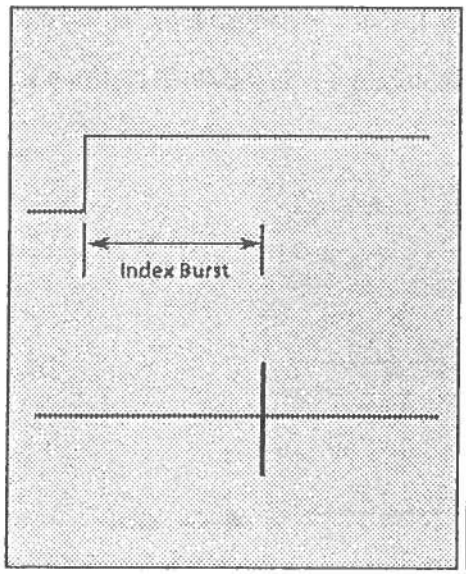


Fig. 9.5 Index Timing

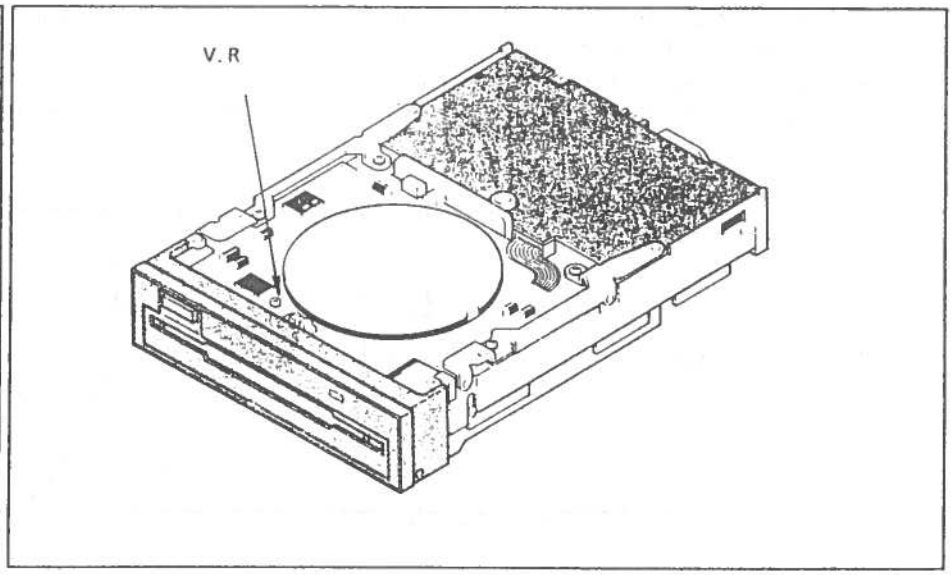


Fig. 9.6 I/B Adjustment

9.9 Track 00 Sensor Adjustment

[In the case of JU-252A/JU-253A]

(1) Set the oscilloscope as follows.
Set horizontal deflection to 1ms/division.

CH1 : ZP
EXT : SP

(2) Step between specified tracks as shown in the FLAG 0 item of Table 8.1 (Turn the seek delay switch on the exerciser to adjust 12 ms seek.)
(3) Loosen the track 0 sensor screw and adjust until the waveform on the oscilloscope appears as shown in Fig. 9.7.

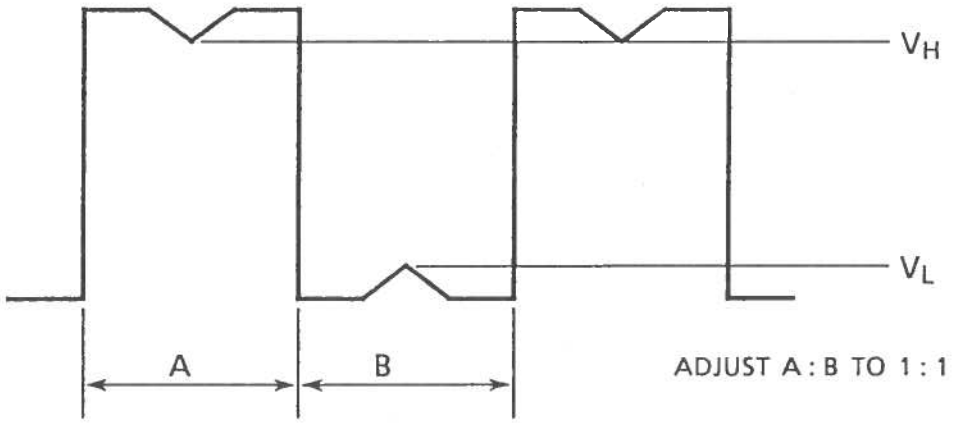


Fig. 9.7 Track 0 Waveform

[In the case of JU - 257 - P/-PF)

[1] Set the oscilloscope as follows.

Set horizontal deflection to 1ms/division.
CH1 : Step (No. 20 Pin of CMOS/TTL Adaptor)
CH2 : ZP

(2) Step between specified tracks as shown in the FLAG0 item of **Table 8.1,** (Turn the seek delay switch on the exerciser to adjust 3 ms seek.)
(3) Loosen the screw for track 0 assembly so that the waveform on the osciloscope is as shown in **Figure 9.8** and adjust the track 0 assembly position by moving it back and forth.

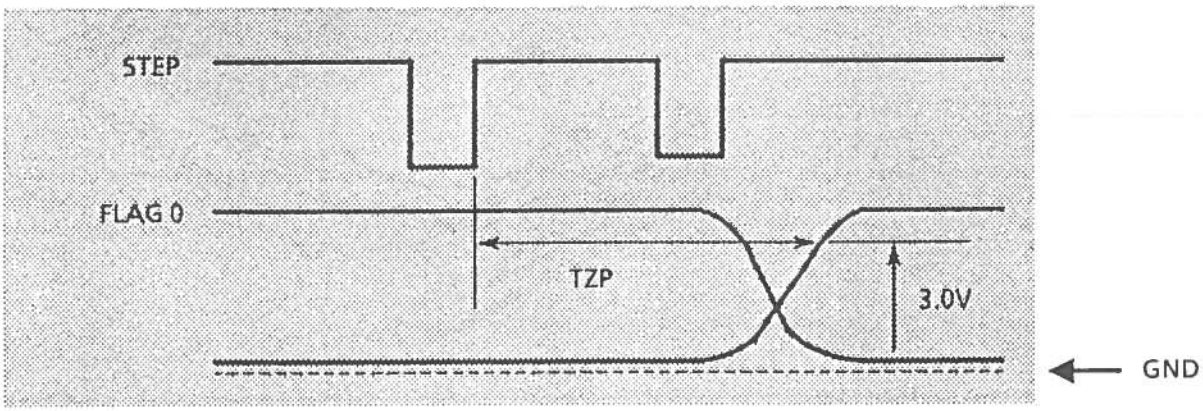


Fig. 9.8 Track 0 Waveform

(4) Voltages/Timings for track 0 waveform

1. T_{ZP}	4.0 ± 1.2 ms

(5) After performing adjustment on items 1 reconfirm the following :
① Recalibrate to track Ø
② Step in for 40 steps.
③ Check the alignment waveform.

9.10 Asymmetry Verification

(1) Insert a data diskette.
(2) Step to the track specified in the Asymmetry item of **Table 8.1.**
(3) Set the oscilloscope as follows:

CH1 : Read Data (No. 30 Pin of CMOS/TTL Adaptor)
CH2 : T1

Set time base to 1μs/division and vertical deflection to 0.2 v/division.

(4) Write 1F.
(5) A read wave form is displayed on the oscilloscope as shown in **Fig. 9.9.**
(6) Confirm if it satisfies the value as shown in **Table 8.1.**

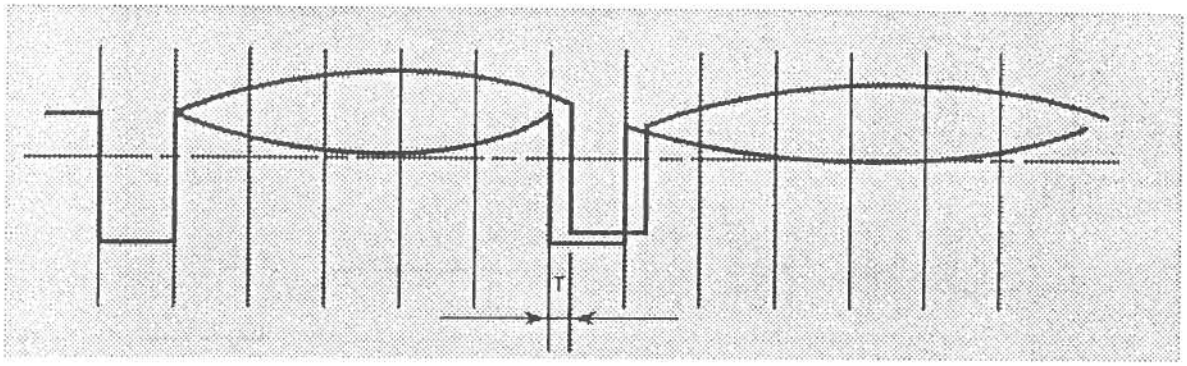
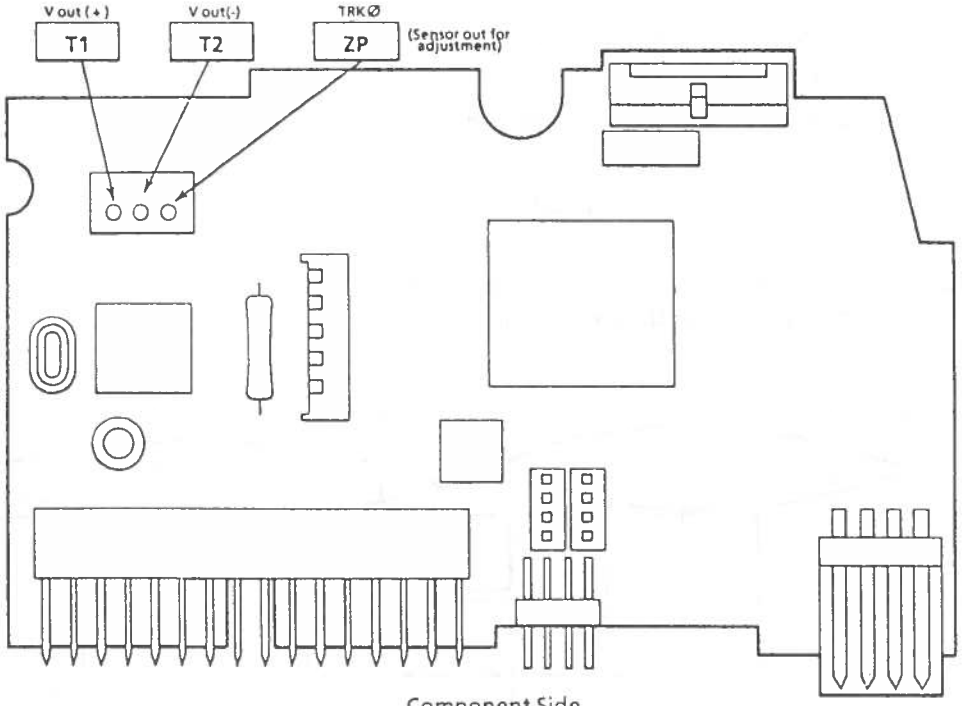


Fig. 9.9 Asymmetry Waveform

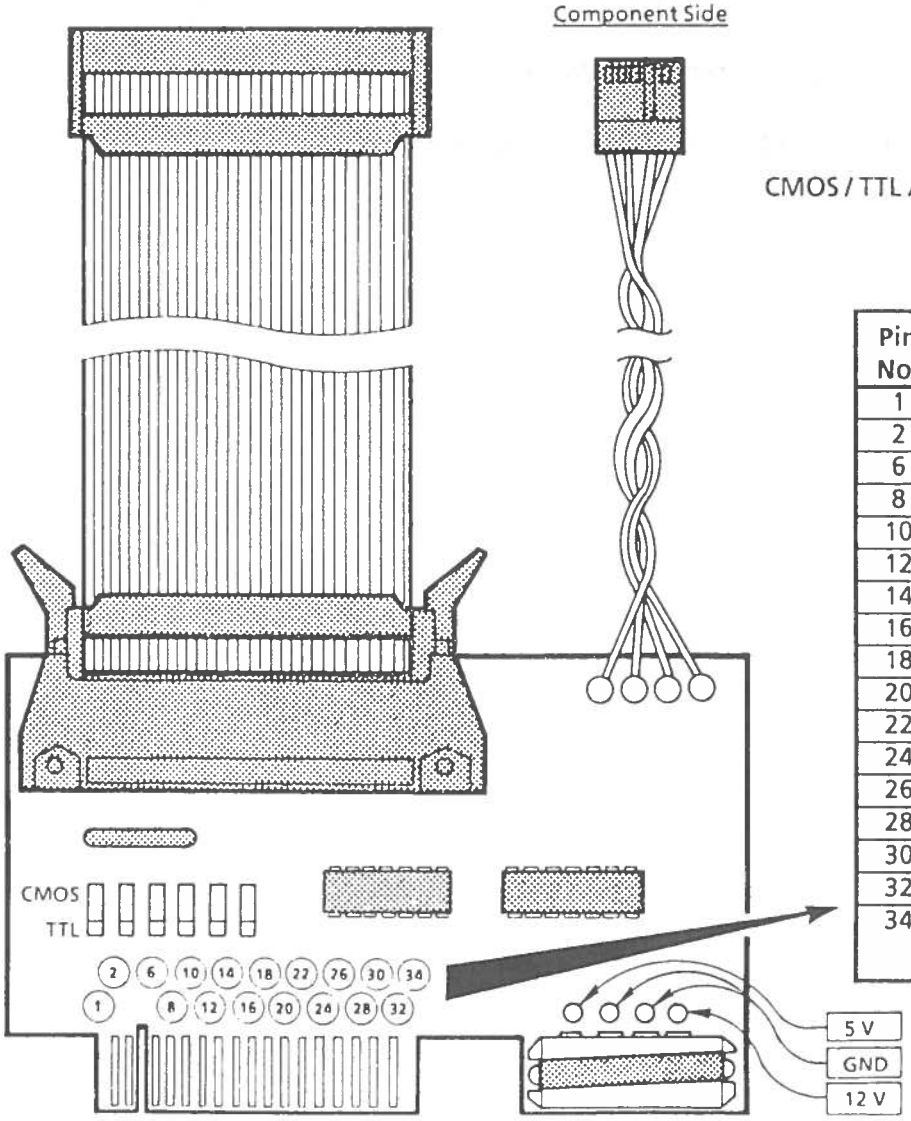
(Asymmetry Wave form might be reversed up-and-down from model to model.)

10. TEST POINTS



Component Side

CMOS / TTL Adaptor [YTFDD - CN35]



Pin No.	Signal
1	NC (Disk Change Reset)
2	Disk Change (Disk In)
6	Drive Select 3
8	Index
10	Drive Select 0
12	Drive Select 1
14	Drive Select 2
16	Motor On
18	Direction Select
20	Step
22	Write Data
24	Write Gate
26	Track 00
28	Write Protect
30	Read Data
32	Side Select
34	Ready (Disk In/Disk-change)

11. PANASONIC ALIGNMENT DISKETTE

3.5 inch Alignment Diskette

Table 11.1

TPI	TYP of Alignment Diskette	P/N		Index Burst	Azimuth	Radial Alignment	MODEL
67.5	DAD	JU-01AA		20TRK	20TRK	20TRK	JU-31X
	CE	817-363CE					
135	DAD	JU-01AA		40TRK	40TRK	40TRK	JU-32X JU-36X JU-323A JU-363A JU-252A JU-253A JU-253-T JU-253-P/-PK
	CE	817-363CE					
135	DAD	817-384		40TRK	40TRK	40TRK	JU-38X JU-39X JU-257-P/-PF

PART. 2 [JU-255-P/-PK]
12. DISASSEMBLY AND REASSEMBLY

12.1 Removing and Remounting the Cover

(1) Remove two cover setscrews.
(2) Disengage the cover from the claws in the four corners of the base and then remove the cover.
(3) Mount the cover in the sequence of (2) to (1) in the above.

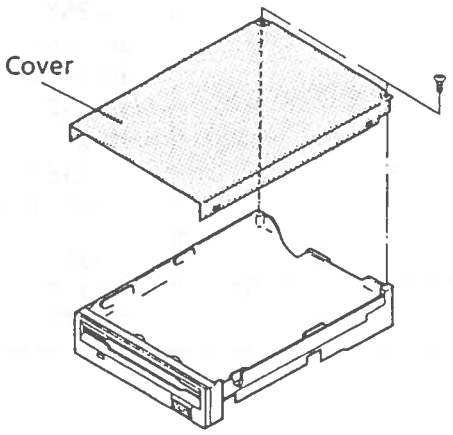


Fig. 12-1. Removing the Cover

12.2 Removing and Remounting the Front Panel Assembly

(1) Remove two front-panel setscrews and remove the front cover.
(2) Remount the front panel in the reverse procedure of step (1) so that the button is inserted into the button hole in the front panel.

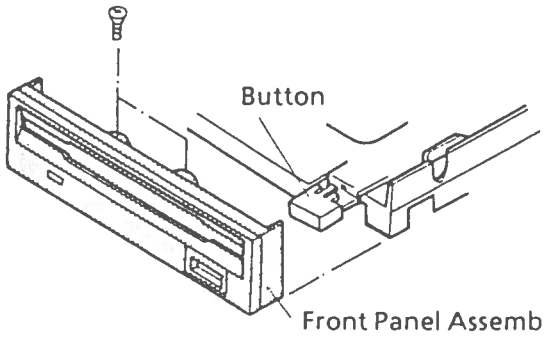


Fig. 12-2. Removing the Front Panel Assembly

12.3 Removing and Remounting the Holder Assembly and Rollers

(1) Remove the cover and front panel in the manners described in sections 12.1 and 12.2.
(2) Press the eject button to its full stroke so that the roller section of the holder assembly can be easily ejected.
(3) Lift the holder assembly by hands and gently slide it toward you, then the four roller sections on the holder will be removed from the eject levers. (Keep in mind that the rollers drop easily.) In this case, when the side 1 of the head assembly drops from the holder, it strikes the head on the side 0 being pushed by the side 1 head retaining spring, so lift it lightly by the thumb.
(4) Remove the four rollers from the holder assembly.
(5) Remount the rollers and holder assembly in the reverse procedure of steps (1) to (4).

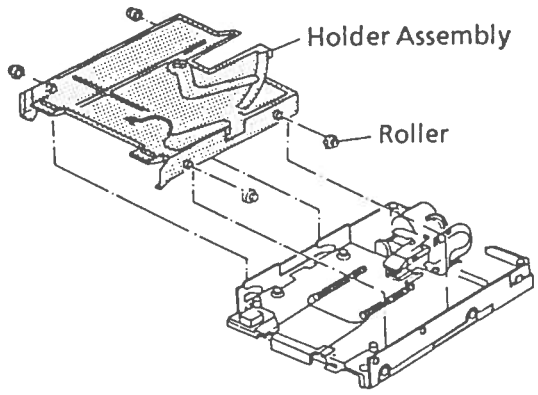


Fig. 12-3. Removing the Holder Assembly and Rollers

12.4 Removing and Remounting the Head FPC, Track 0 Connector, and Stepper Motor Connector

(1) Draw the contact section of the head FPC upwards out of the head connector J6 by pinching it by flat pens with care not to damage it.
(2) Remove the track 0 cable connector (red) from the connector J3 (on the stepper motor side, red) on the PCB.
(3) Remove the stepper motor cable connector (brown) from the connector J4 (on the track 0 side, brown).

(4) Remount the above in the reverse procedure of steps (1) to (3).
In this case, be sure to insert the head FPC to the full extent in the right angle. Wiring should be made so that the lead wire of the track 0 and the stepper motor does not contact the carriage of the head or hang over the track 0.
(5) Ensure that the head FPC is not higher than the track 0 assembly.
(6) Ensure that the head FPC does not contact the head of the track 0 assembly set screw.

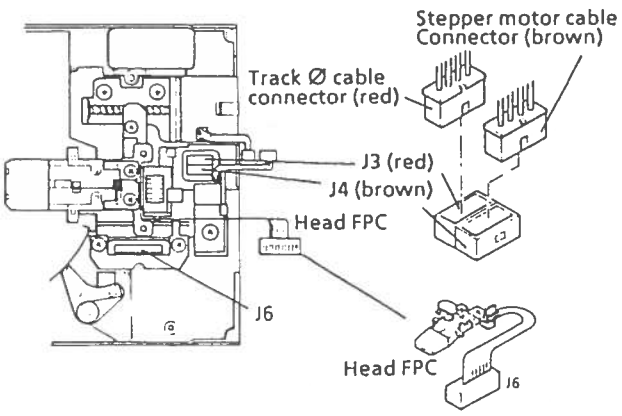


Fig. 12-4. Removing the Head FPC, Track 0 Connector, and Stepper Motor Connector

12.5 Removing and Remounting the Head Carriage Assembly, Rod Clamp, and Guide Rod

(1) Remove the holder assembly according to the procedure in section 12.3.
(2) Remove the head FPC from the connector J6 according to the procedure in section 12.4.
(3) Remove two set screws on the rod and remove the rod clamp.
(4) Move the head carriage assembly in the reverse direction of the stepper motor (rightward) and remove it.
(5) Draw the guide rod out of the head carriage assembly.
(6) Remount the above in the reverse procedure of steps (1) to (5).

[Cautions for Remounting]

(7) Apply oil to the guide rod (but not too much), insert the rod into the head assembly, move it back and forth several times, and confirm that the guide rod moves smoothly.
(8) Place the position where the head carriage assembly pinches the stepper motor lead screw at the center of the lead screw length.
(9) Place the mounting position of the guide rod on the base so that the tail end of the guide rod comes to the same position as the base or projected less than 1 mm.
(10) After remounting the above, adjust the radial alignment according to the procedure in section 9.6, adjust the track 00 sensor according to the procedure in section 9.9.

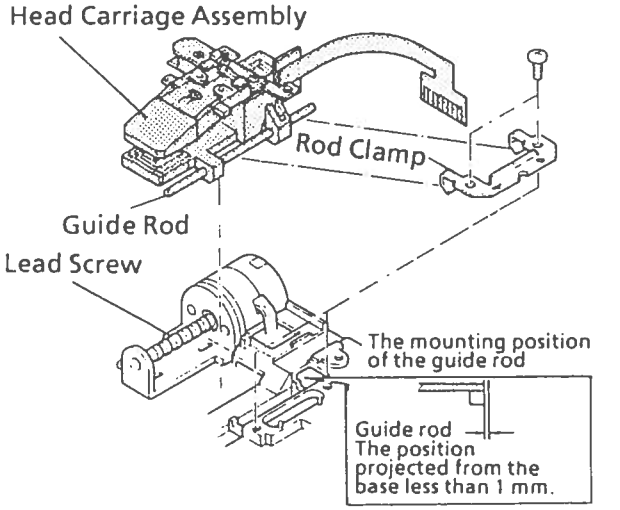


Fig. 12-5. Removing the Head Carriage Assembly, Rod Clamp, and Guide Rod

12.6 Removing and Remounting the Track 0 Assembly

(1) Remove the cover according to the procedure in section 12.1.
(2) Remove the track 0 cable connector according to the procedure in section 12.4.
(3) Remove the set screw on the track 0 assembly and remove the track 0 assembly.
(4) Remount the track 0 assembly in the reverse procedure of steps (1) to (3).
(5) After remounting track 0 assembly, adjust the track 00 sensor according to the procedure in 9.9.

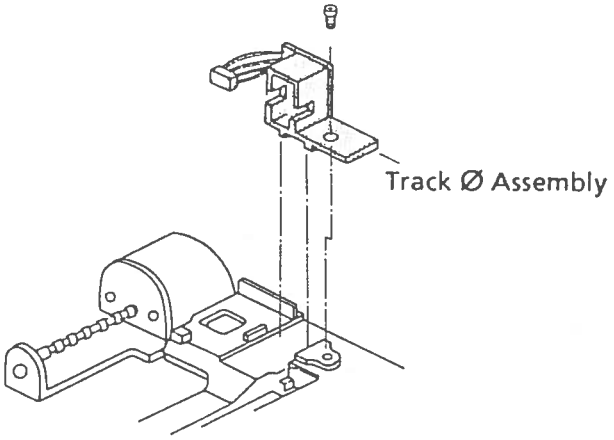


Fig. 12-6. Removing Track 0 Assembly

12.7 Removing and Remounting the Stepper Motor

(1) Remove the cover according to the procedure in section 12.1.
(2) Remove the stepper motor cable connector according to the procedure in section 12.4.
(3) Remove the two set screws on the stepper motor and remove the stepper motor.
(4) Remount the stepper motor in the reverse procedure of steps (1) to (30).
(5) Ensure that the temporary fastened position of the stepper motor is placed so that the two projections on the base come to the centers of the two long holes in the stepper motor respectively.
(6) Apply* grease to the lead screw of the stepper motor according to the procedures in steps (7) and (8).
(7) Put grease in the size of a grain of rice on the lead screw.
(8) Extend the grease over the lead screw evenly using an applicator.
(9) After remounting the stepper motor, adjust the radial alignment according to the procedure in section 9.6, adjust the track 00 sensor according to the procedure in section 9.9.

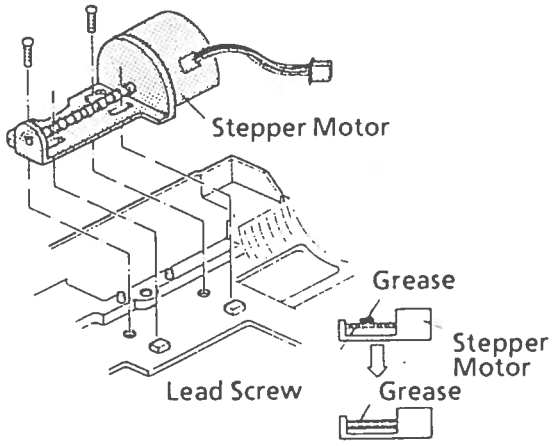


Fig. 12-7. Removing the Stepper Motor

12.8 Removing and Remounting the Trigger Lever Assembly

(1) Remove the cover according to the procedure in section 12.1.
(2) Remove the trigger lever set screws and remove the trigger lever spring and trigger lever assembly.
(3) Remount the above in the reverse procedure of steps (1) and (2).

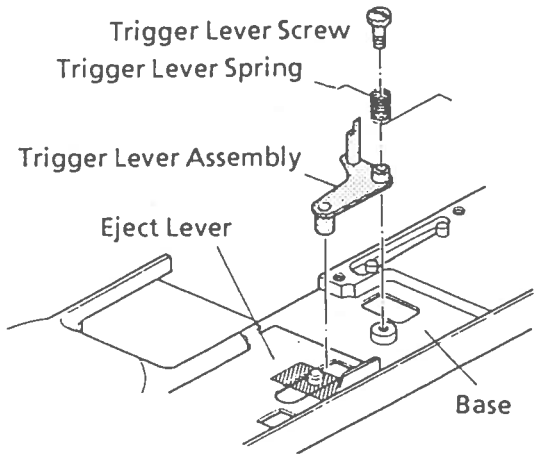


Fig. 12-8. Removing the Trigger Lever Assembly

12.9 Removing and Remounting the Eject Lever Springs

(1) Remove the holder assembly according to the procedure in section 12.4.
(2) Remove the hook of the eject lever spring and remove the eject lever spring.
(3) Remount the eject lever spring in the reverse procedure of steps (1) and (2).

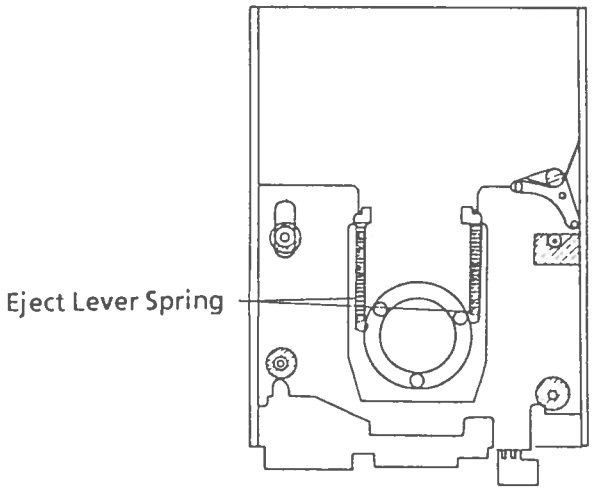


Fig. 12-9. Removing the Eject Lever Spring

12.10 Removing and Remounting the Eject Lever

(1) Remove the eject lever springs according to the procedure in section 12.9.
(2) Remove the trigger lever assembly according to the procedure in section 12.8.
(3) Remove the four stopper rings and washers from the eject lever.
Each stopper ring has a slit, so it can be easily removed by pinching the portion adjacent to the slit by tweezers.
(4) Remove the eject lever.
(5) Remount the eject lever in the reverse procedure of steps (1) to (4).

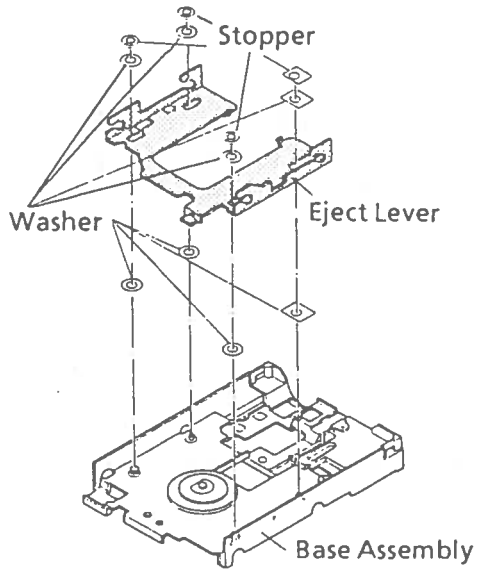


Fig. 12-10. Removing the Eject Lever

12.11 Removing and Remounting the Microswitch Assembly

(1) Remove the holder assembly according to the procedure in section 12.3.
(2) Remove the three soldered portions of the microswitch assembly lead wires on the D motor PC board.
(3) Remove the microswitch assembly set screw and remove the microswitch assembly.
(4) Remount the microswitch assembly in the reverse procedure of steps (1) to (3).
(5) Observe the instructions in the following table when soldering the three lead wires onto the D motor PC board.

No. on the D motor PC board	Color of lead wire
1	Yellow
2	White
3	Blue

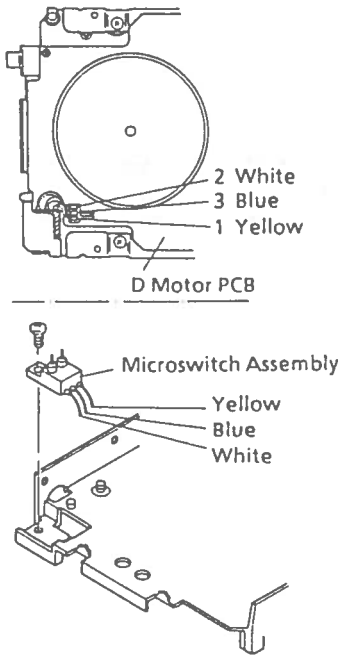


Fig. 12-11. Removing the Microswitch Assembly

12.12 Removing and Remounting the Mounting Brackets

(1) Remove the four screws on the right and left side bracket assemblies and remove the right and left side bracket assemblies.
(2) Remount the bracket in the reverse procedure of step (1) with care not to pinch the D motor cable by the mounting bracket.

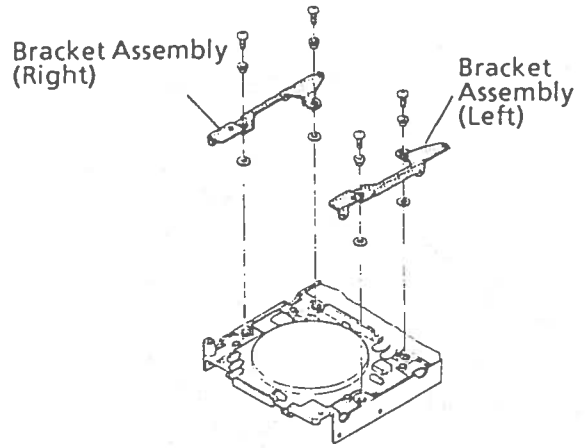


Fig. 12-12. Removing the Mounting Bracket

12.13 Removing and Remounting the Control PC Board

(1) Remove the mounting bracket according to the procedure in section 12.12.
(2) Remove the head FPC, trackØ connector, and stepper motor connector according to the procedure in section 12.4.
(3) Remove the three set screws from the control PC board.
(4) Remove the D motor PC board socket housing from the connector J5 and remove the control PC board.
(5) Remount the control PC board in the reverse procedure of steps (1) to (4).
(6) Treat the cable in the D motor PC board socket housing as shown in figure 12-15.

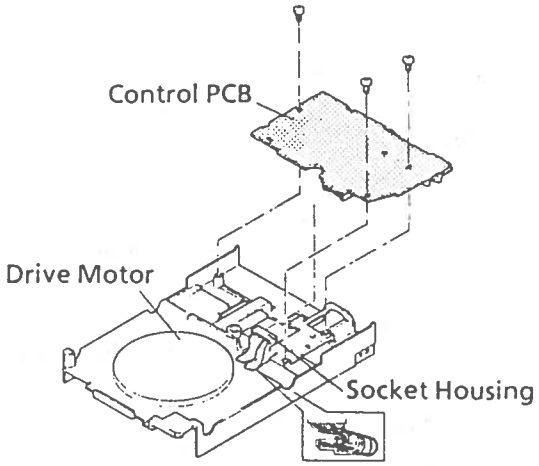


Fig. 12-13. Removing the Control PC Board

12.14 Removing and Remounting the Drive Motor Assembly

(1) Remove the holder assembly according to the procedure in section 12.3.
(2) Remove the control PC board according to the procedure in section 12.13.
(3) Remove the microswitch assembly according to the procedure in section 12.11.
(4) Remove the three front (head side) drive motor set screws.
(5) Remove the three back (PC board side) drive motor set screws and remove the drive motor assembly.

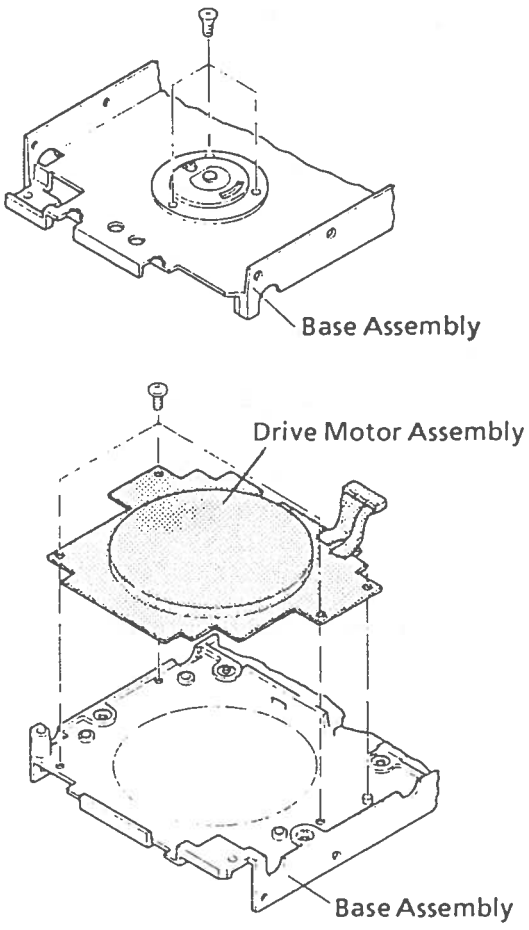


Fig. 12-14. Removing the Drive Motor Assembly

12.15 Disassembling and Reassembling the Mounting Bracket Assembly

(1) Press the collar bracket from beneath the mounting bracket assembly with a minus screwdriver, then the collar bracket and washer are removed from the holes in the mounting bracket.
(2) Reassemble the mounting bracket assembly in the reverse order of step (1).

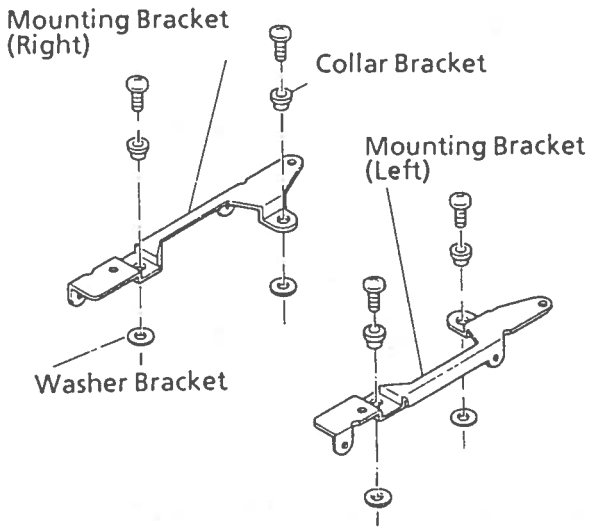


Fig. 12-15. Disassembling the Mounting Bracket

12.16 Removing and Remounting the Pushbutton

(1) Pull down the pushbutton with its hook and remove the pushbutton from the eject lever. Push Ⓐ with flat blade screwdriver while pulling out.
(2) Remount the pushbutton in the reverse procedure of step (1).

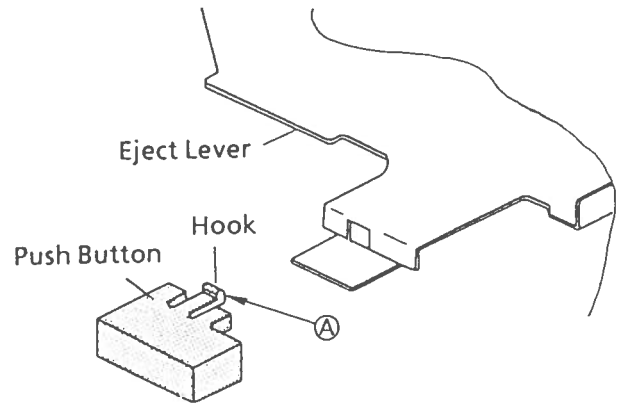


Fig. 12-16. Removing the Pushbutton

12.17 Disassembling and Reassembling the Holder Assembly

(1) Remove the hooks of the shutter lever spring from the shutter lever assembly and from the holder.

(2) Move the shutter lever assembly in the arrow direction in the figure riding across the stopper until it reaches the dotted line position, remove the shutter lever assembly with the tab on the holder aligned with the hole, and remove the shutter lever spring from the holder.

(3) Remove the reverse insertion preventive lever spring from the tab.

(4) Move the reverse insertion preventive lever until it reaches the dotted line position and remove it with the tab on the holder aligned with the hole.

(5) Reassemble the holder assembly in the reverse procedure of steps (1) to (4).

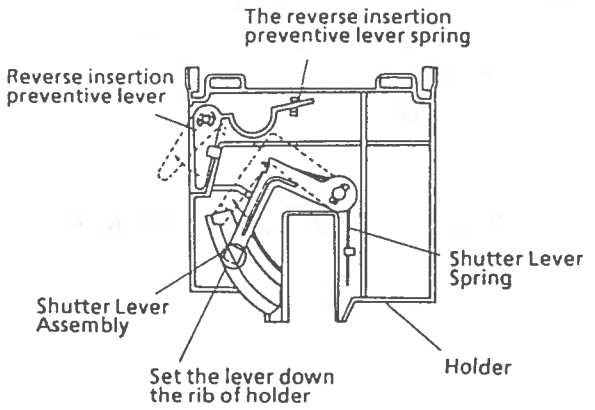


Fig. 12-17. Disassembling the Holder Assembly

12.18 Mounting the Drive Motor LED

(1) Solder the LED in the position indicated in figure 12-18.

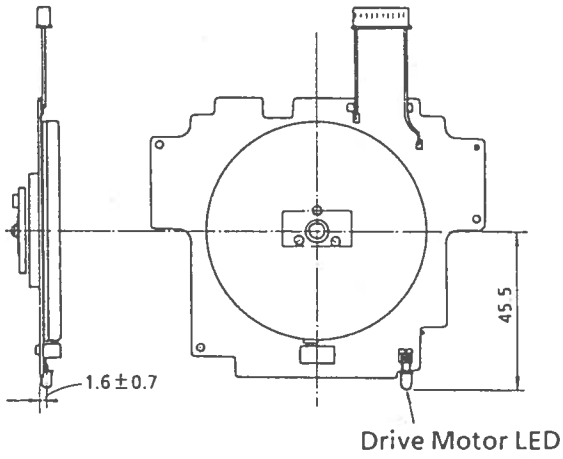


Fig. 12-18. Mounting the Drive Motor LED

12.19 Removing and Remounting of the Damper

(1) Remove the cover according to the procedure in section 12.1.

(2) Remove the two damper mounting screws and remove the damper with care not to give excessive force to the carriage arm.

(3) Remount the damper in the reverse procedure of steps (1) and (2).

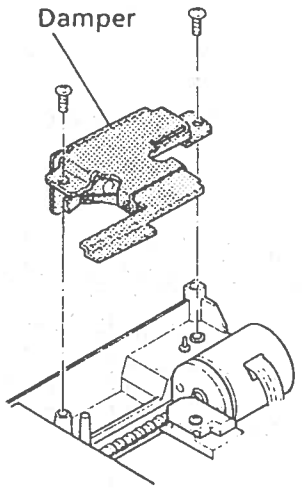


Fig. 12-19. Removal of the Damper

12.20 Removing and Remounting of the HD Switch

(1) Remove the front panel according to the procedure in section 12.2.
(2) Remove the lead wire from the D motor board side using a soldering iron.
(3) Remove the HD switch fastening screw and remove the HD switch.
(4) Remount the switch in the reverse procedure of steps (1) to (3).

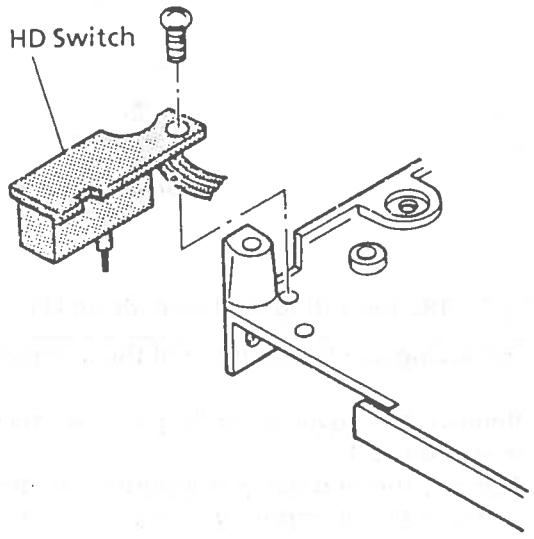


Fig. 12-20. Removal of the HD Switch

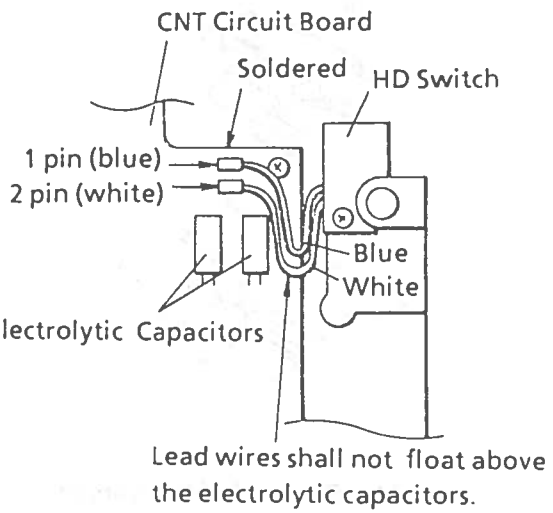


Fig. 12-20.1 Soldering of HD Switch Lead Wire

12.21 Disassembly and Reassembly of the Damper

(1) Remove one of the hanger shaft fastening clamp E rings.
(2) Remove the hanger shaft from the hanger bracket section and remove the hanger spring and arm.
(3) Remove the two damper fastening screws and remove the damper.
(4) Reassemble the damper in the reverse order of steps (1) to (3).

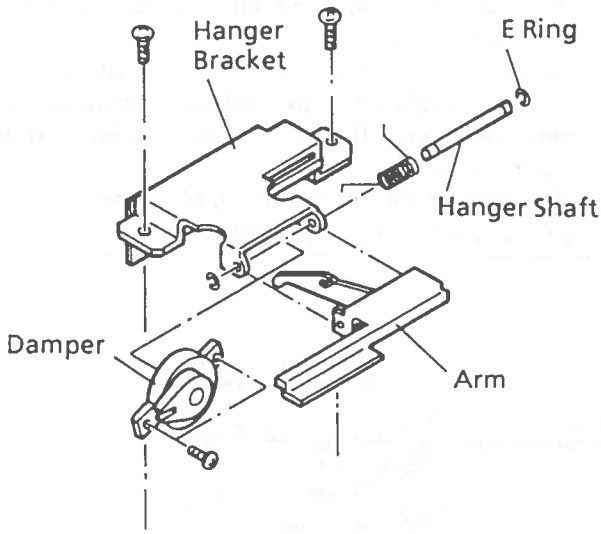
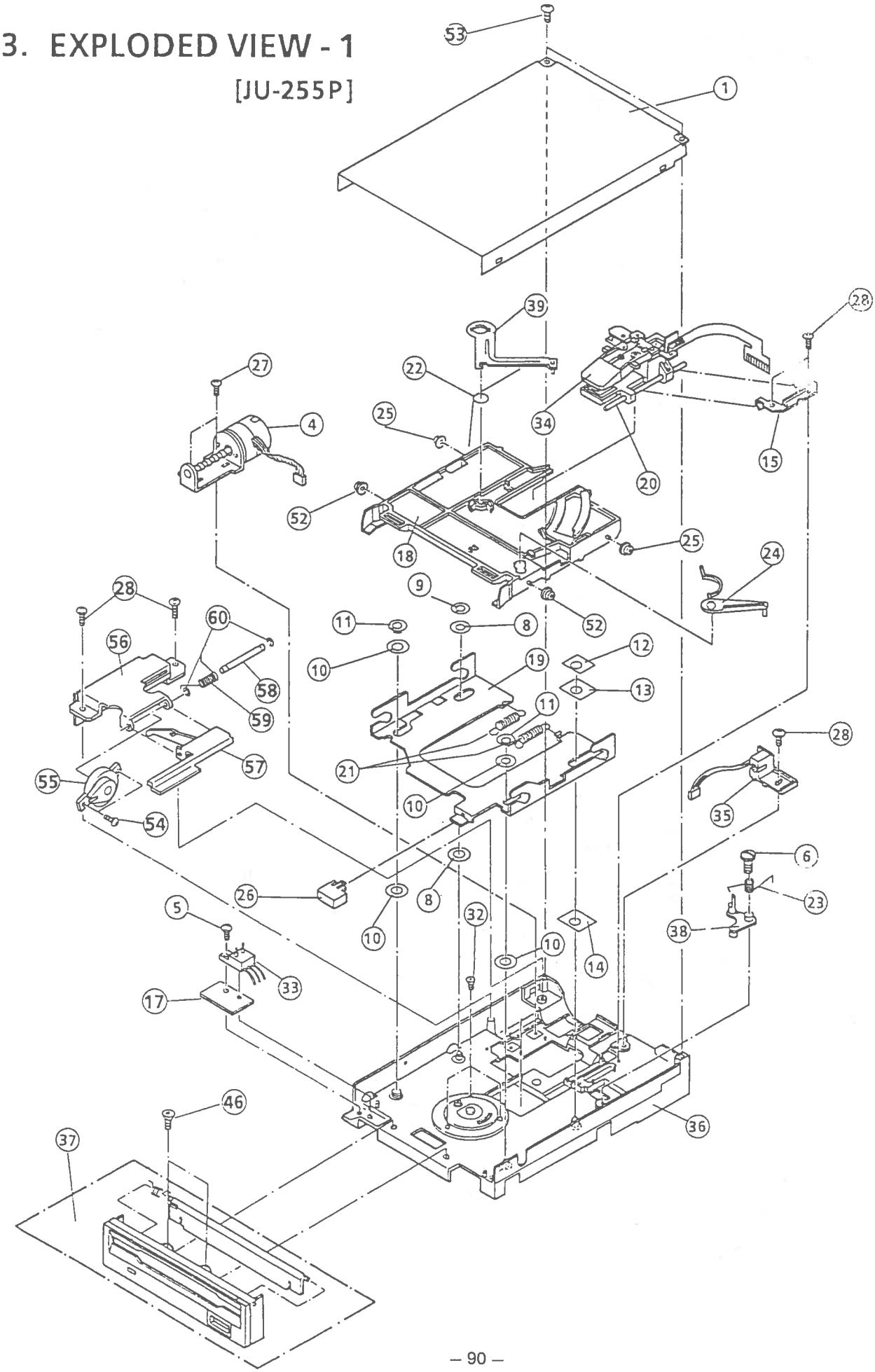


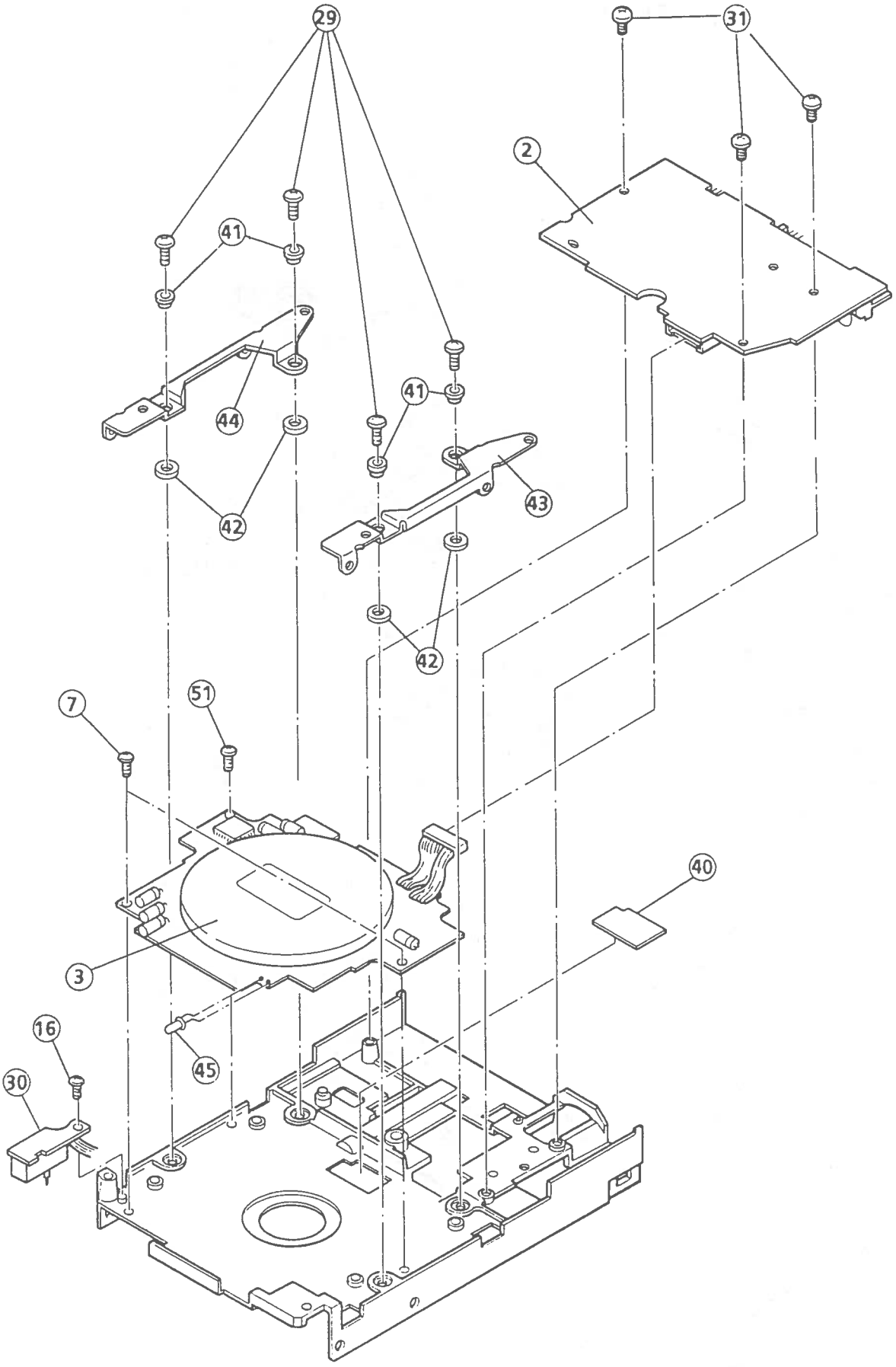
Fig. 12-21 Disassembly of the Damper

13. EXPLODED VIEW - 1

[JU-255P]



EXPLODED VIEW - 2 [JU-255-P]



14. PARTS LIST

Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price N.R. Yen (¥) (FOB: JAPAN)	Rank
1	0007 8540	Cover	YTF2K08240B3	1			C
2	0007 8541	Control PCB ass'y	YTUF255PK-CN	1			A
3	0007 8542 (0007 8543)	Drive motor	YTUF35DMTJ-5 YTFMD02300B4)	1			A
4	0007 8544	Stepper motor	YTFMD02552B4	1			A
5	0007 8545	Screw (for Micro switch ass'y)	YTF1E00941B4	1	5		C
6	0007 8546	Screw (for Trigger lever)	YTF1E00702B4	1	5		C
7	0007 4086	Screw (for Drive motor PCB)	YTF1E00770B4	2	5		C
8	0007 4087	Washer 06	YTF1K00121B4	2	5		C
9	0007 4088	Stopper 05.6	YTF1K00171B4	1	5		C
10	0007 4089	Washer C	YTF1K00370B4	4	5		C
11	0007 4090	Stopper C	YTF1K00390B4	2	5		C
12	0007 4091	Stopper F	YTF1K00530B4	1	5		C
13	0007 4092	Washer	YTF1K00760B4	1	5		C
14	0007 4151	Washer B	YTF1K00363B4	1	5		C
15	0007 8547	Clamp (for Guide rod)	YTF2C08060B4	1	5		C
16	0007 4084	Screw (for HD screw ass'y)	YTF1E00550B4	1	5		C
17	0007 8548	Spacer (for Micro switch ass'y)	YTF2N08670B4	1	5		C
18	0007 8549	Holer	YTF2K0737AB2	1			C
19	0007 8550	Eject lever	YTF2K07830B3	1			C
20	0007 8551	Guide rod	YTF4H03730B4	1			C
21	0007 8552	Spring (for Eject lever)	YTF4J03790B4	2	5		C
22	0007 8553	Spring (for Shutter lever)	YTF4J02543B4	1	5		C
23	0007 8554	Spring (for Trigger lever)	YTF4J02661B4	1	5		C
24	0007 8555	Lever (Prevented incorrect insertion)	YTF4R02553B4	1	5		C
25	0007 8556	Roller	YTF4S03620B4	2	5		C
26	0007 8557	Button (for Eject)	YTF6J03460B4	1	5		C
27	0007 4106	Screw (for Stepper motor)	YTF1E00990B4	2	5		C
28	0007 4107	Screw [Clamp (2), TRK 0 ass'y (1), Damper ass'y (2)]	XSB25+4FX	5	5		C
29	0007 4108	Screw (for Bracket)	XSB25+6FX	4	5		C
30	0007 8558	HD switch ass'y	YTUF255HDSW	1			B
31	0007 8559	Screw (for Control PCB)	XSB25+3FX	3	5		C
32	0007 4111	Screw (for Drive motor)	XSS2+4FX	3	5		C
33	0007 8560	Micro switch ass'y	YTUF253DET4	1			A
34	0007 8561	Head ass'y	YTUF255PHD	1			A

Note: ☆ – New parts
Q'ty– Quantity used per unit
* – Minimum order and supply quantity

Rank A: Essential
B: Stock recommended
C: Others
X: No stock recommended

Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price N.R. Yen (¥) (FOB: JAPAN)	Rank
35	0007 4114	Track 0 ass'y	YTUF253TR0	1			B
36	0007 8562	Base ass'y	YTF7K08482B3	1			X
37	0007 8563	Front panel ass'y (Including shutter)	YTF7K08560B3	1			A
38	0007 8564	Trigger lever ass'y	YTF7K08831B4	1			C
39	0007 8565	Shutter lever ass'y	YTF7K09210B4	1			C
40	0007 8566	Shield plate	YTF2H08260B4	1	5		C
41	0007 4120	Collar (for Bracket)	YTF2P05910B4	4	5		C
42	0007 4121	Washer (for Bracket)	YTF2P05921B4	4	5		C
43	0007 4122	Bracket (Left)	YTF2S05560B4	1			C
44	0007 4123	Bracket (Right)	YTF2S05550B4	1			C
45	0007 4658	LED (on Motor PCB)	LN28RP	1	5		B
46	0007 8567	Screw (for Front panel)	YTX1E01400B4	2	5		C
51	0007 8568	Screw (for Drive motor PCB)	YTF1E01241B4	1	5		C
52	0007 8569	Roller	YTF4S03740B4	2	5		C
53	0007 4614	Screw (for Cover)	XSN2+5FX	2	5		C
54	0007 8570	Screw (for Damper)	YTF1E01220B4	2	5		C
55	0007 8571	Damper	YTF2F06700B4	1			C
56	0007 8572	Hanger bracket	YTF2S08100B3	1			C
57	0007 8573	Hanger	YTF4A03531B3	1			C
58	0007 8574	Hanger shaft	YTF4H02990B4	1	5		C
59	0007 8575	Hanger spring	YTF4J03610B4	1	5		
60	0007 8576	Retaining ring	XUC12V	2	5		C
L3, 4	3013 0133	Low frequency coil	NL322522-101	2			B
L5	0007 8500	Low frequency coil	NL322522-221	1			B
L7	0007 4567	Choke coil	SN-3-2002	1			B
IC1	0007 4182	IC (Stepper)	HA13421AMP	1			A
IC2	0007 8501	IC	FQL00401B4	1			A
IC3	0007 4572	LSI (R/W)	HA16651MP	1			A
VR1	0007 4187	Variable resistor	EVMUGA00B24	1			B
X1	0007 8502	Oscillator	EFO-FC4004A4	1			B
CN1	0007 8503 (0007 4193	Connector	YT08050705 FCN-725P034)	1			X
CN2	0007 4194	Connector (Power)	171826-4	1			X
CN	0007 8504	Connector	YTFJC00760B4	1			X
CN5	0007 8505	Connector	FJC00620B410	1			X
CN4	0007 4199	Connector	FJC00401B402	1	5		X
CN3	0007 4200	Connector	FJC00401B409	1	5		X

Note: ☆ — New parts
Q'ty — Quantity used per unit
* — Minimum order and supply quantity

Rank A: Essential
B: Stock recommended
C: Others
X: No stock recommneded

Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price N.R. Yen (¥) (FOB: JAPAN)	Rank
CN6	0007 4201	Connector	FJC00410B407	1			X
L6	0007 8506	High frequency coil (Ferrite beads)	FBA03HA450KD	1	5		C
CN	0007 8507	Short plug	IMSA-9215H-T	2	5		C
IC4	0007 8508	IC	DN74LS16-1SA	1			A
IR1	0007 8509	Block resistor	NIKRD8-134	1			C
C15	0007 8510	Chip capacitor	FCC00510B122	1	5		C
C9	0007 8511	Chip capacitor	FCC00510B181	1	5		C
C16	0007 8512	Chip capacitor	FCC00510B391	1	5		C
C6	0007 8513	Chip capacitor	FCC00510B821	1	5		C
L9	0007 8514	Low frequency coil	NL322522-330	1			C
R20	0007 8515	Chip resistor	MCR18EZHG183	1	5		C
R12	0007 8516	Chip resistor	MCR18EZHG511	1	5		C
R17	0007 4243	Chip resistor	MCR18EZHG682	1	5		C
R6	0007 8517	Chip resistor	MCR18EZHJ103	1	5		C
R55	0007 4597	Chip resistor	MCR18EZHJ392	1	5		C
R13	0007 4216	Chip resistor	MCR18EZHJ473	1	5		C
R4	0007 8518	Chip resistor	MC100JZHJ152	1	5		C
D11	0007 8519 (0007 4586	Diode	MA151WA-TX DAP202KT-96)	1			C
C2	0007 8520	Chip capacitor	FCC00510B121	1	5		C
C3	0007 8521	Chip capacitor	FCC00510B621	1	5		C
C1	0007 8522	Chip capacitor	FCC00550B104	1	5		C
C13, 14	0007 8523	Chip capacitor	FC00560B103	2	5		C
C5, 7, 11, 17	0007 8524	Chip capacitor	UMK325F474Z	4			C
C8	0007 8525	Chip capacitor	FCC00510B101	1	5		C
R47, 54	0007 6213	Chip resistor	MCR10EZHJ102	2	5		C
R41~43, R56~58, R59,90,91, 93	0007 4214	Chip resistor	MCR18EZHJ393	10	5		C
R10,14,13	2792 0831	Chip resistor	MCR10EZHJ103	3	10		C
R11	0007 4216	Chip resistor	MCR18EZHJ473	1	5		C
R30	0007 4217	Chip resistor	MCR18EZHJ331	1	5		C
R24, 51	0007 4218	Chip resistor	MCR18EZHJ751	2	5		C
R27, 28	0007 4219	Chip resistor	MCR18EZHJ561	2	5		C
R32,39,40, 49,50, 96, 97	0007 6217	Chip resistor	MCR10EZHJ393	7	5		C

Note: ☆ — New parts
Q'ty — Quantity used per unit
* — Minimum order and supply quantity

Rank A: Essential
B: Stock recommended
C: Others
X: No stock recommneded

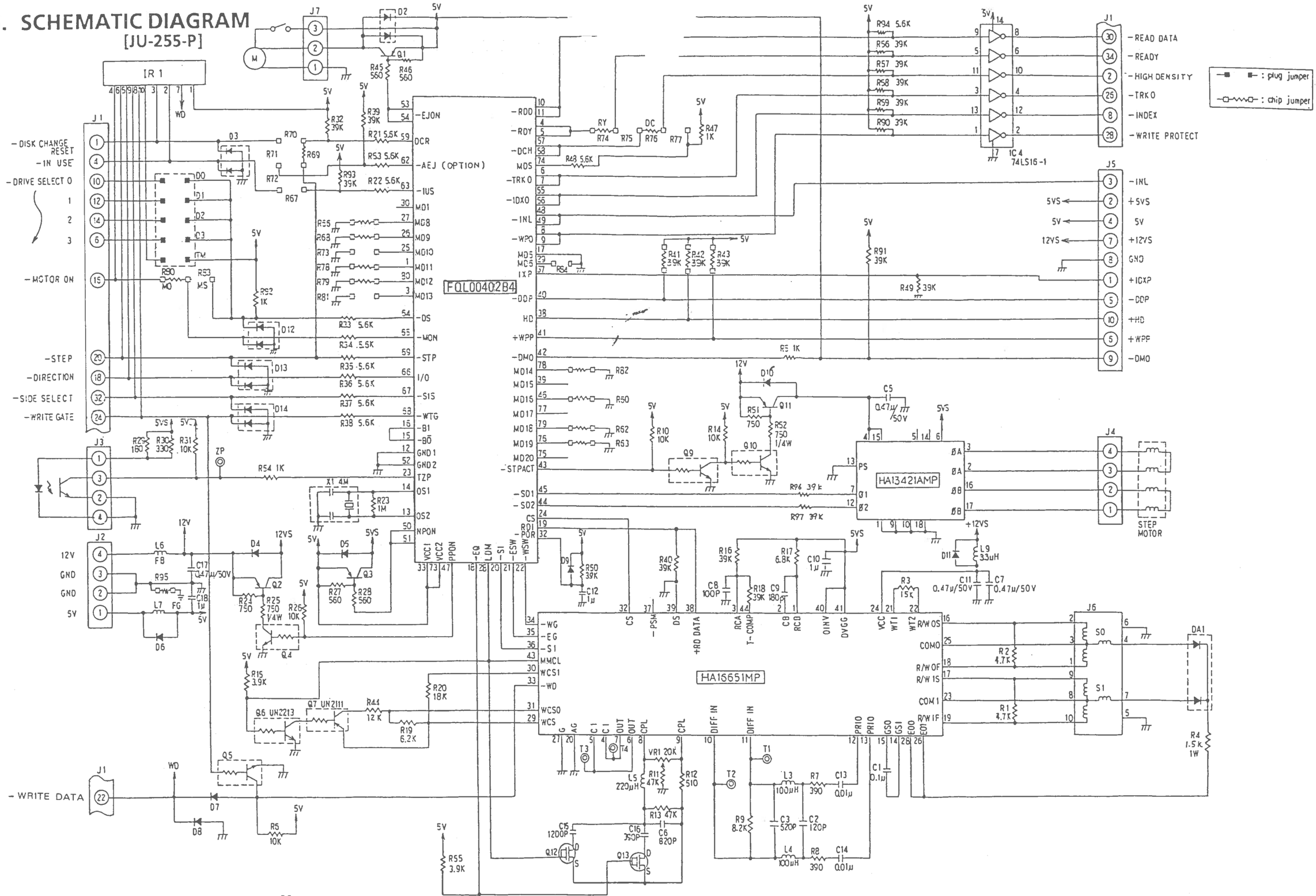
Item	Code No.	Parts Name	Specification	Q'ty	*	Unit Price N.R. Yen (¥) (FOB: JAPAN)	Rank
R21,22, 33~38, 48,53,94	2792 1108	Chip resistor	MCR10EZHJ562	11	5		C
R44	0007 8526	Chip resistor	MCR18EZHG123	1	5		C
R3	0007 4223	Chip resistor	MCR18EZHG153	1	5		C
R7, 8	0007 4221	Chip resistor	MCR18EZHG391	2	5		C
R60,62,63, 66,68,69, 74,76, 78~80, 82,95	0007 4173	Chip resistor	MCR18EZHJ000	13	5		C
D7	0007 4229	Diode	MA704-TW	1	5		C
Q2	0007 8527	Transistor	2SB1114T2BZL	1			A
Q3, 11	0007 4237	Transistor	2SB766-TW	2			A
C10,12,18	0007 8528	Chip capacitor	FCC00500B105	3			C
R16, 18	0007 4598	Chip resistor	MCR18EZHG393	2	10		C
R1, 2	0007 4174	Chip resistor	MCR18EZHG472	2	5		C
R26	0007 4245	Chip resistor	MCR18EZHJ103	1	5		C
R19	0007 8529	Chip resistor	MCR18EZHG622	1	5		C
R23	0007 4605	Chip resistor	MCR18EZHJ105	1	5		C
R9	0007 4555	Chip resistor	MCR18EZHG822	1	5		C
R29	0007 4601	Chip resistor	MCR18EZHJ181	1	5		C
R5, 92	2792 0314	Chip resistor	MCR18EZHJ102	2	10		C
R15	2792 0349	Chip resistor	MCR18EZHJ392	1	10		C
Q5	0007 4239	Transistor	UN2215-TW	1	5		A
D3~6, 8~10, 12~14	0007 3372 (0007 8530	Diode	MA151WA-TW DAP202KT-97)	10			C
D1	0007 8531 (0007 8533	Diode	MA151WK-TW DAN202KT-97)	1			C
Q7	0007 8533 (0007 8534	Transistor	UN2111-TW DTA114EKT-97)	1	5		A
R25, 52	0007 8535	Resistor	MCR25JZHJ751	2	5		C
Q12, 13	0007 8536	Transistor	3SK144R-TX	2			A
Q4, 10	0007 3367 (0007 8537	Transistor	UN2211-TW DTC114ETK-97)	2			A
Q6, 9	0007 8538 (0007 8539	Transistor	UN2213-TW DTC144EKT-97)	2	5		A

Note: ☆ — New parts
Q'ty — Quantity used per unit
* — Minimum order and supply quantity

Rank A: Essential
B: Stock recommended
C: Others
X: No stock recommended

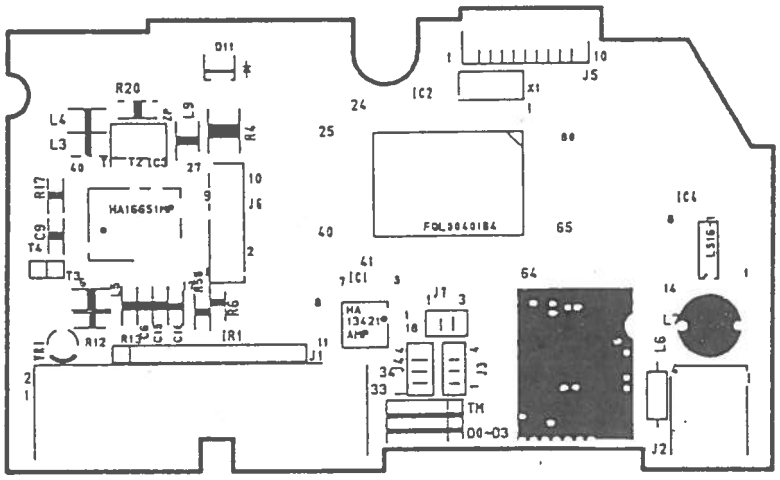
15. SCHEMATIC DIAGRAM

[JU-255-P]

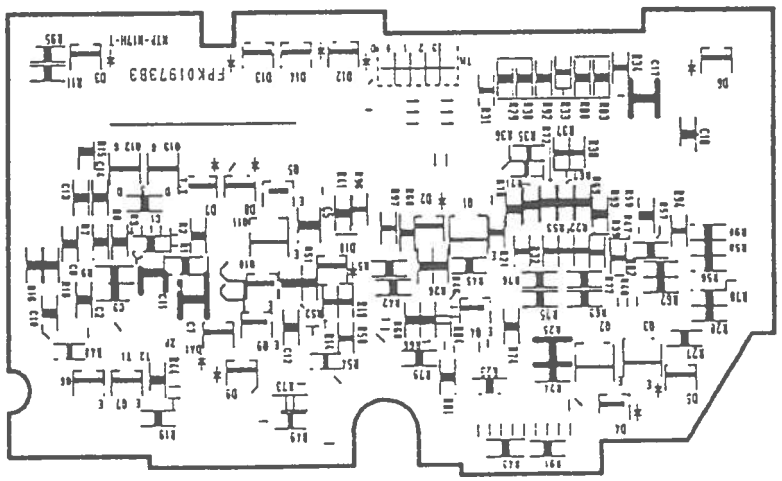


16. CIRCUIT BOARD [JU-255-P]

Component Side (Top)



Solder Side (Bottom)



Wave Memory RAM address from CPU

Wave Memory RAM address from GAA

Wave Memory RAM address output

Select Wave Memory RAM address either from CPU or GAA

Control signals from GAB

DACs' volume control for MIX

16-bit digital sound signal to DAC(B)

Wave Memory RAM data bus

16-bit digital sound signal to DAC(A)

Outputs digital sound signals alternately to DAC(A) and DAC(B)

Wave Memory RAM data bus

Wave Memory RAM (2 megabytes)

Bidirectional Bus Buffer

CPU data bus

GAS-2

JPD65012G -282-12

GAX

MB653121

M74F04N X10

M51038 X2

F04-2(1/6)x2

LS245-4

LS245-3

TC74HC04P

HC08-2

M52228 X2

TC511000P-10-9

TC511000P-10-10

TC511000P-10-11

TC511000P-10-12

TC511000P-10-13

TC511000P-10-14

TC511000P-10-15

TC511000P-10-16

TC511000P-10-8

TC511000P-10-7

TC511000P-10-6

TC511000P-10-5

TC511000P-10-4

TC511000P-10-3

TC511000P-10-2

TC511000P-10-1

CPU
μpD70216

Interrupt from GAS

Interrupt from I/O Port

MIDI IN

MIDI OUT

8MHz clock

Bidirectional Bus Buffer

Bidirectional Bus Buffer

Address Latch

Address Latch

Address Latch

System RAM 1
μpD43256C-1

System ROM 1
μpD27C256AD-12MZ3B

System RAM 2
μpD43256C-2

System ROM 2
μpD23C256AD-12MZ4B

HCT244-1

System ROM/RAM Chip Selector

Chip Selector

Controls External Port, FDC, GAB, and GAA

I/O Port 1
μpD71055C-1

I/O Port 2
μpD71055C-2

Decoder

- GAS, FDC, control
- Switch scaning
- Gain control for recording

NORM, GAIN, FOOT SW

R

168~218 (μpD71055)

A0~15

FOOT SW

SCI

EBB

SCO~3

HC154

SIO~7

μPD71055

2MHz

DO~15

A1, A2

PCMINT

DMARQI

BMWR

BMRD

WREB

REF

ASTB

UBE

DMAAKI

SCSI1

SCSI2

IOWR

IORD

IO2S

IO1S

REFRQ

Vave Memory RAM
ddress control
ia GAS.

DO~7
RAS.MUX (GAS)
TBI~4
PAI~21
SH
EBB

Bus Buffer

HCT244-2

OUT5 LA6462D-4
OUT1 LA6462D-1
OUT6 LA6462D-2
OUT1 LA6462D-3

OUT5
OUT7
OUT1
OUT3
OUT6
OUT8
OUT2
OUT4

DCF 1 (FMI-1)
DCF 2 (FMI-2)
DCF 3 (FMI-3)
DCF 4 (FMI-4)

Digital controlled filter, amplifier.
DCF3 is also used as 9/4.5KHz filter
for 18/9KHz sampling.

HC02, HC368
HC32-2
IM TC40H004P-2
CSA3.58
f = 3.58MHz

A2,4,5
RAS.MUX(GAS)
PAI~21
TBI~4

μPD4053(1/3)-1
μPD4053(1/3)-2
NJM082(1/2)-2
NJM082(1/2)-3

ESH2 100Ω
ESH8 100Ω
ESH1 100Ω
ESH7 100Ω
C823(M)
C331 3.3K

SH1
SH0
SH7
SH6

PCM 54HP(B)
PCM 54HP(A)
HC04

Convert 16-bit digital sound signals into
4channel multiplex wavefrom.

B0~15

FOOT SW
(UPD71055)
R
16B~21B
(UPD71055)
A0~15
RD0~15
RES
NORM.GAIN.FOOT SW

GAS-2
JPD65012G -282-12

Wave Memory RAM
address from CPU

Wave Memory RAM
address from GAA

Wave Memory RAM
address output

Select Wave
Memory RAM
address either from
CPU or GAA

M74F04N X10

Wave Memory RAM data bus

Control signals from GAB

GAX
MB63121

DACs'
volume
control
for MIX

16-bit digital
sound signal
to DAC(B)

Wave Memory
RAM data bus

16-bit digital
sound signal
to DAC(A)

Outputs digital sound signals
alternately to DAC(A) and
DAC(B)

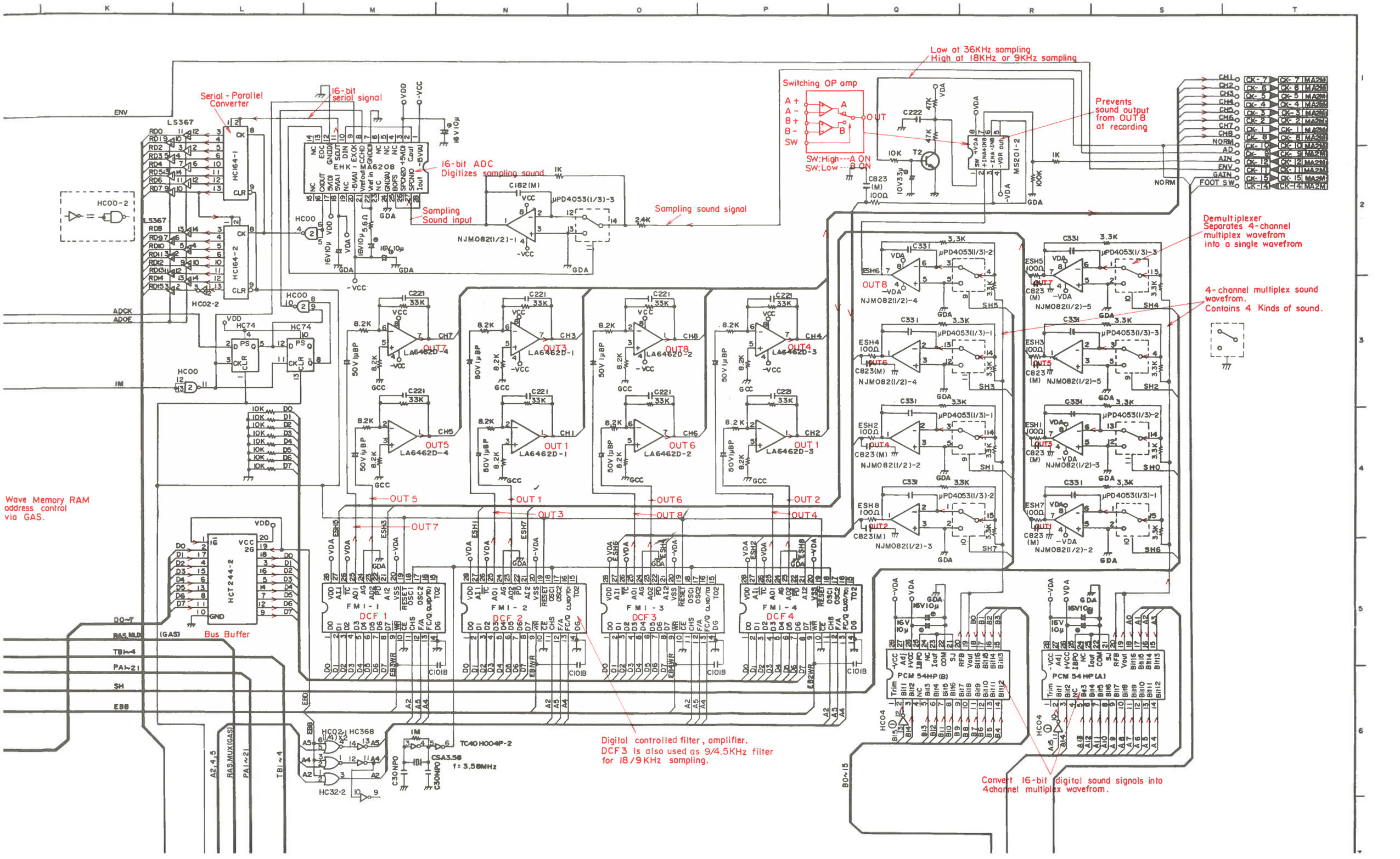
Wave Memory RAM (2 megabytes)

MS2228 X2

+VCC
GCC
-VCC
RSET
VDD
VDA
GDA
-VDA
FG

CD-10 CD-GY P52M
CD-9 CD-O P52M
CD-8 CD-BR P52M
CD-2 CD-W P52M
CD-3 CD-BL P52M
CD-4 CD-Y P52M
CD-7 CD-BK P52M
CD-6 CD-PP P52M
CD-5 CD-GR P52M
CD-1 CD-R P52M

FDD Control Unit
FDC
μPD72067C
LED Latch
LS174
LED WR
Digitize analog value of Master Volume and Value sliders.
Master Volume
Volume
Multiplexer
LCD Control
μPD65012C046 GAL
GAA
μPD65081GF-012
Signal for GAS
Chip select
GAB and GAA interface signals
CPU data bus
Volume control for Mix, Cross Mix
Read Write from CPU
Wave Memory RAM address
RAS MUX(GAS)
CPU
μPD70216
Address Latch
HC373-1
Bidirectional Bus Buffer
Interrupt from GAS
Interrupt from I/O Port
MIDI IN
MIDI OUT
System RAM1
μPD43256C-1
System ROM 1
μPD27C256AD-12M Z38
System RAM2
μPD43256C-2
System ROM 2
μPD23C256AD-12M Z48
System ROM/RAM Chip Selector
Controls External Port, FDC, GAB, and GAA
NORM, GAIN, FOOT SW
FOOT SW
SCI
(μPD71055)
(HC154)


Serial - Parallel Converter
16-bit serial signal
16-bit ADC
Digitizes sampling sound
Sampling Sound input
Sampling sound signal
Switching OP amp
SW:High---A ON
SW:Low---B ON
Low at 36KHz sampling
High at 18KHz or 9KHz sampling
Prevents sound output from OUT8 at recording
Demultiplexer
Separates 4-channel multiplex wavefrom into a single wavefrom
4-channel multiplex sound wavefrom.
Contains 4 Kinds of sound.
Wave Memory RAM address control via GAS.
Bus Buffer
Digital controlled filter, amplifier.
DCF3 is also used as 9/4.5KHz filter for 18/9KHz sampling.
Convert 16-bit digital sound signals into 4channel multiplex wavefrom.
NORM
OUT 1
OUT 2
OUT 3
OUT 4
OUT 5
OUT 6
OUT 7
OUT 8

SCHEMATIC DIAGRAM 1. PCB M5307-MA1M (1/2)